

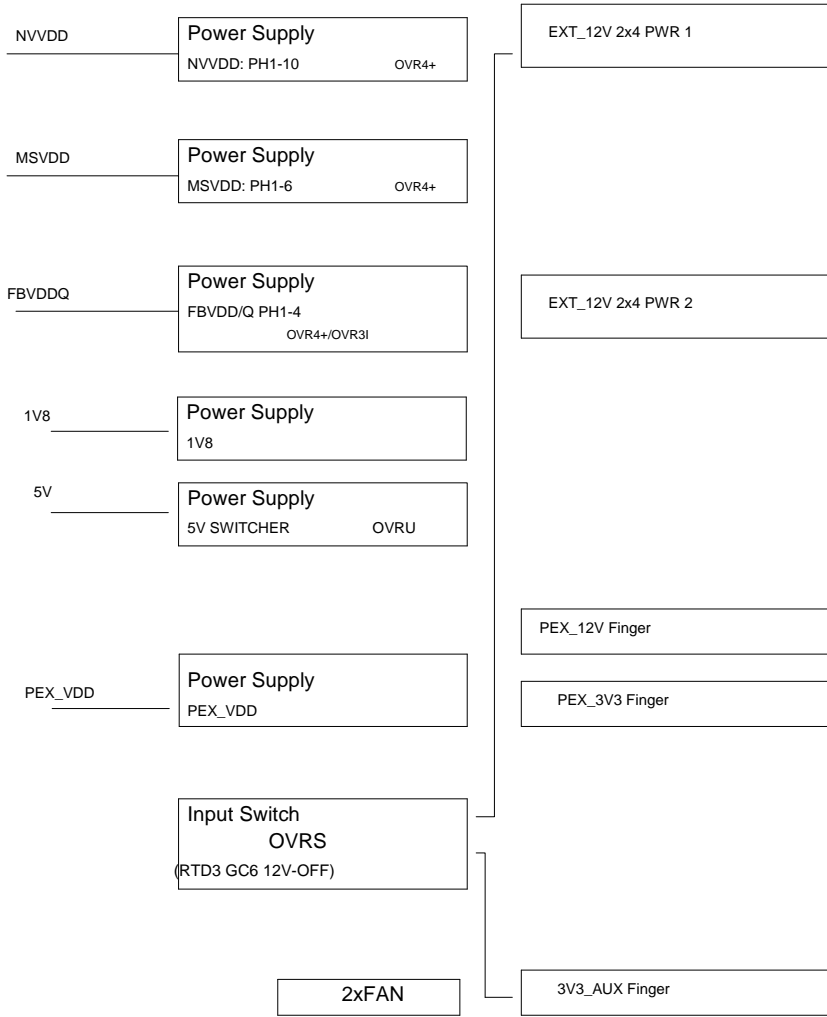
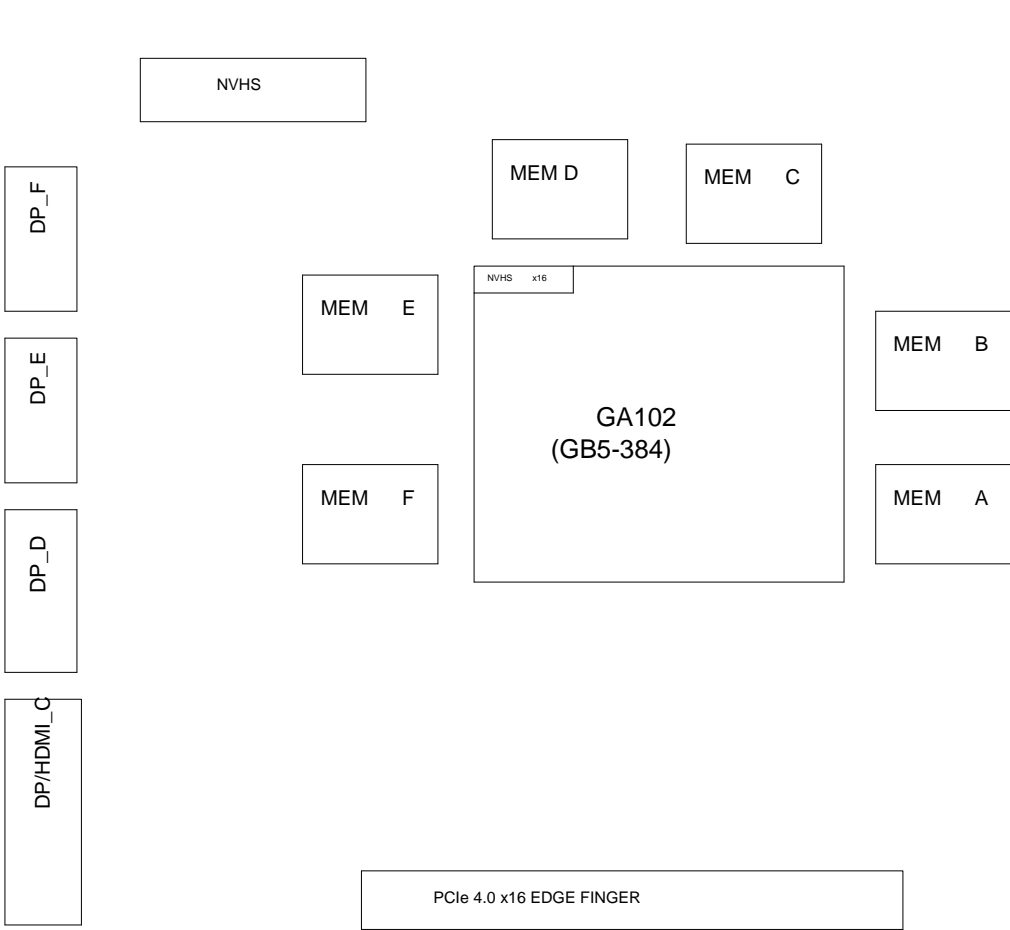
PG132-A02

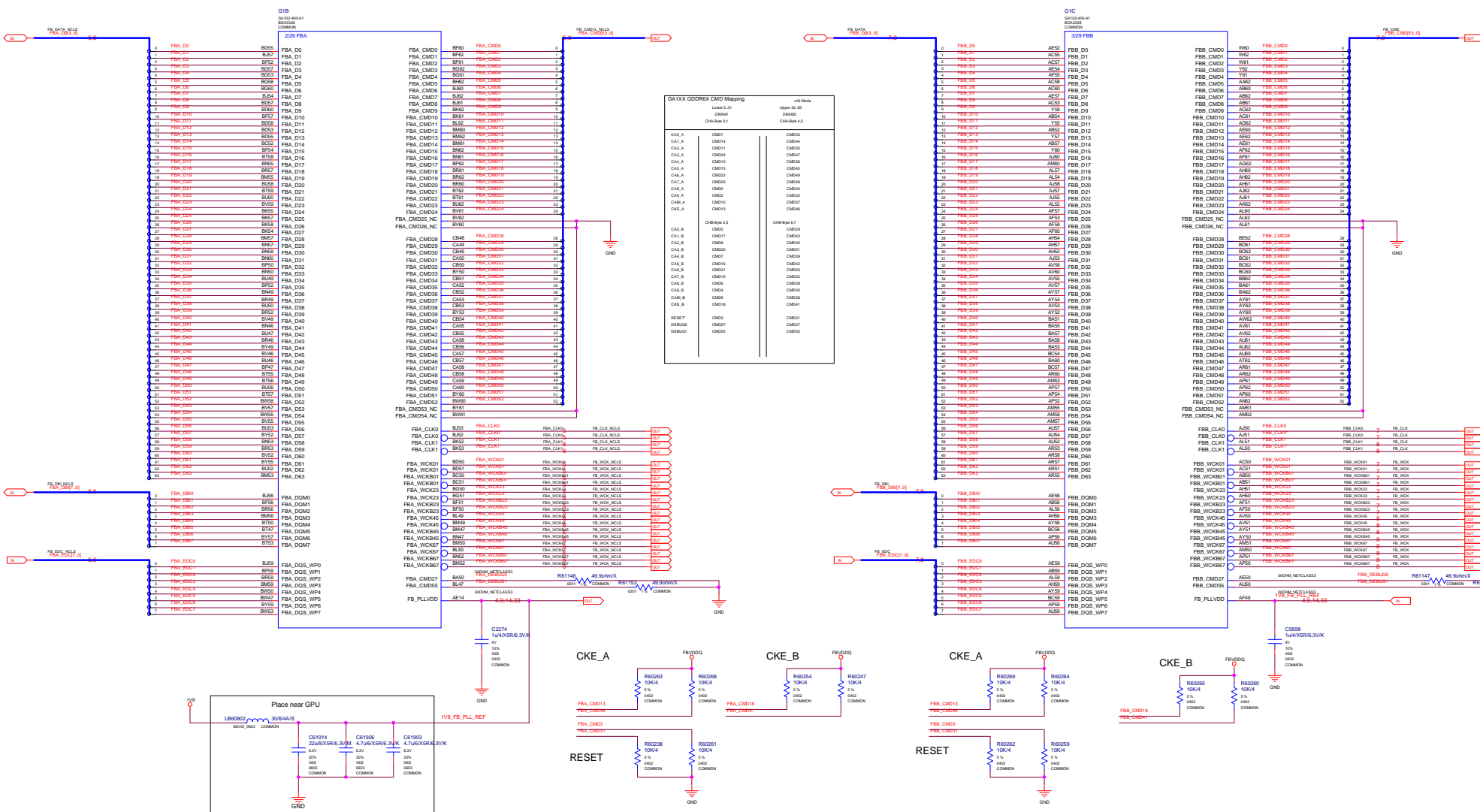
370W, FH Std PCB, 384b, GDDR6x 2CH X16
DP + DP + DP + HDMI/DP

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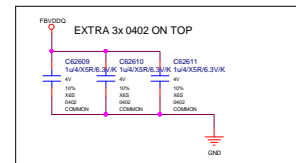
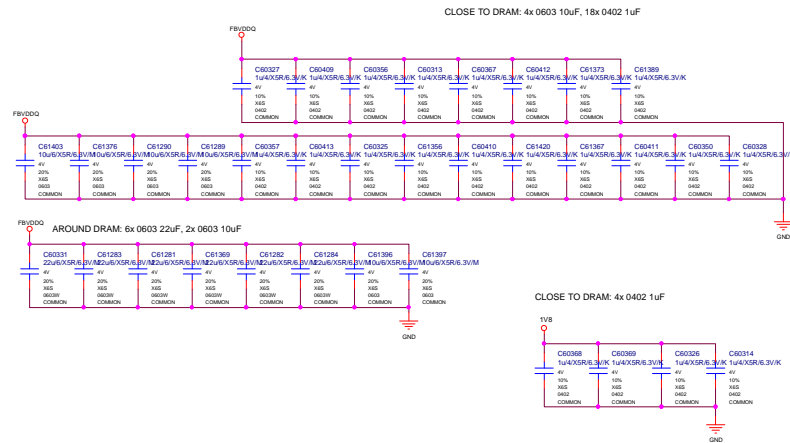
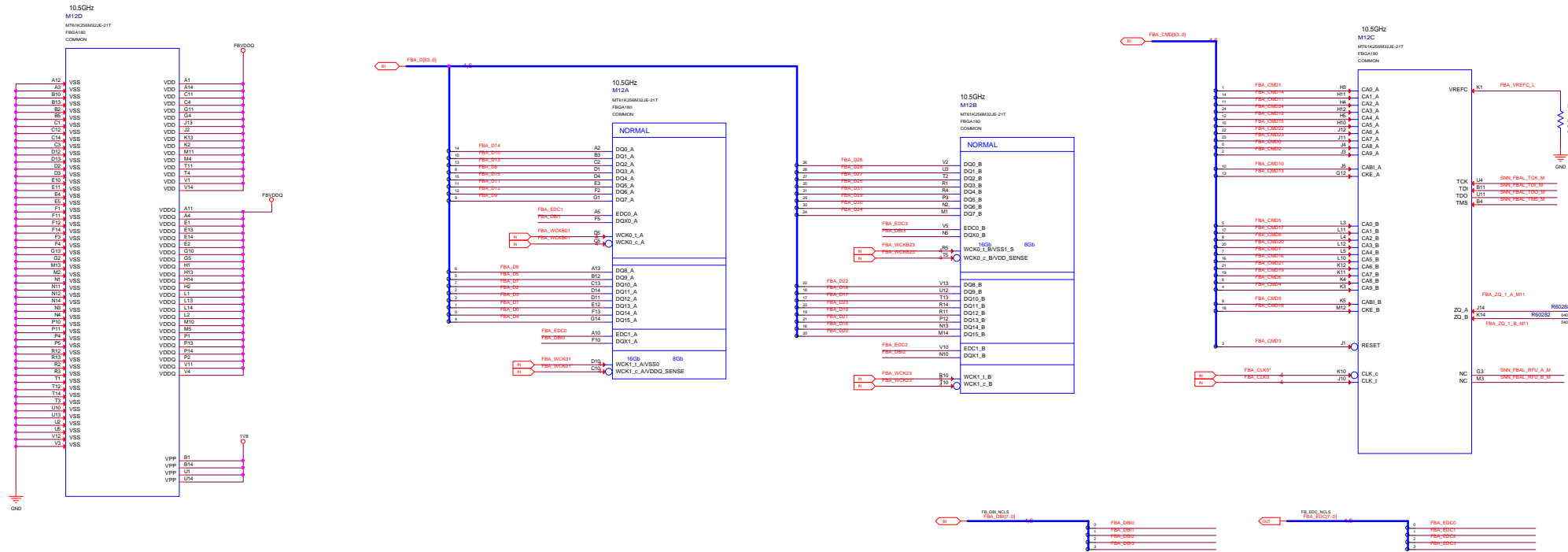
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Block Diagram

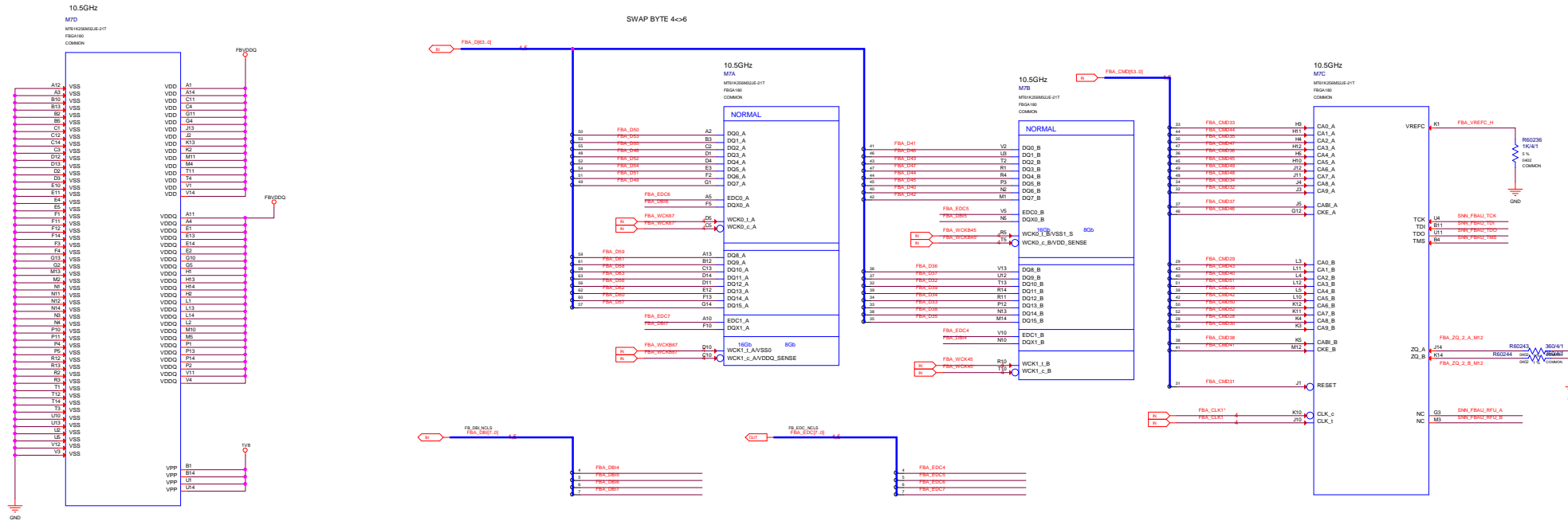




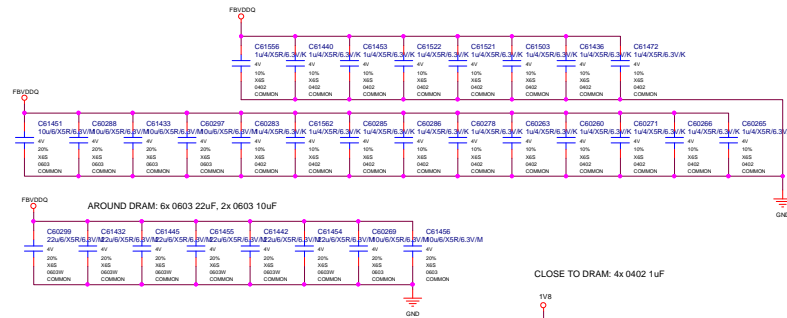
MEMORY: FBA Partition 31..0



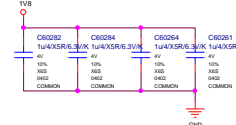
MEMORY: FBA Partition 63..32



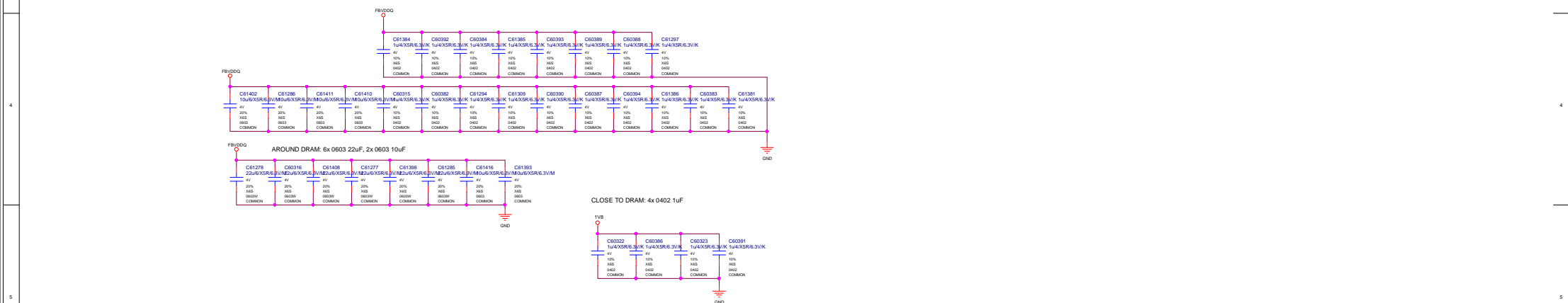
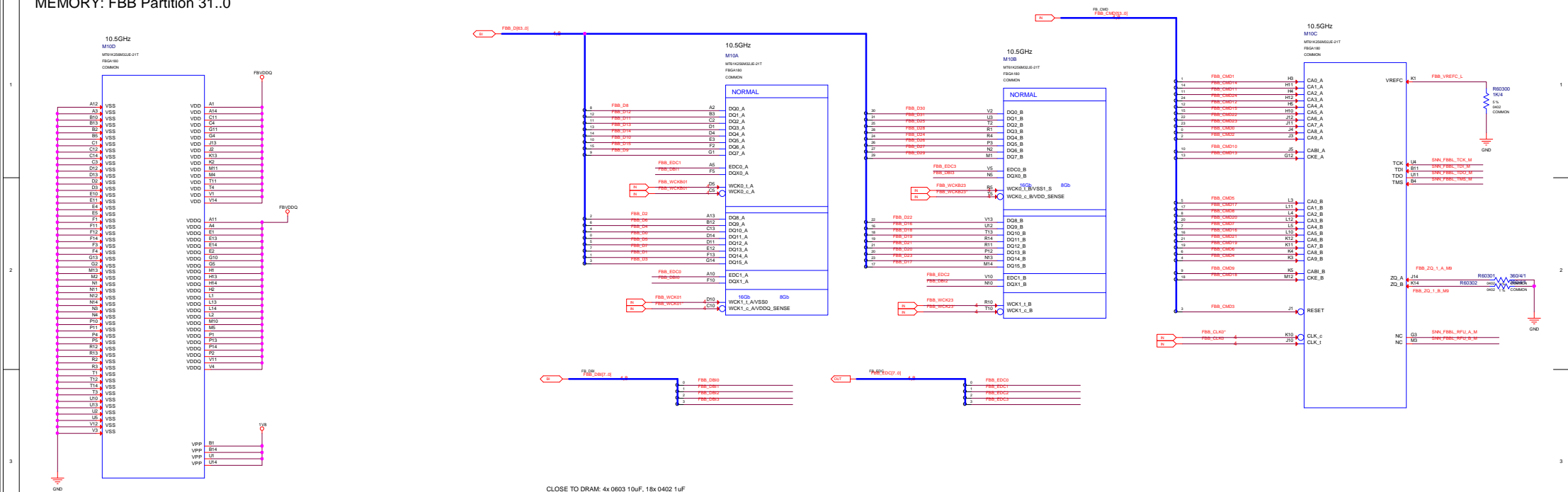
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



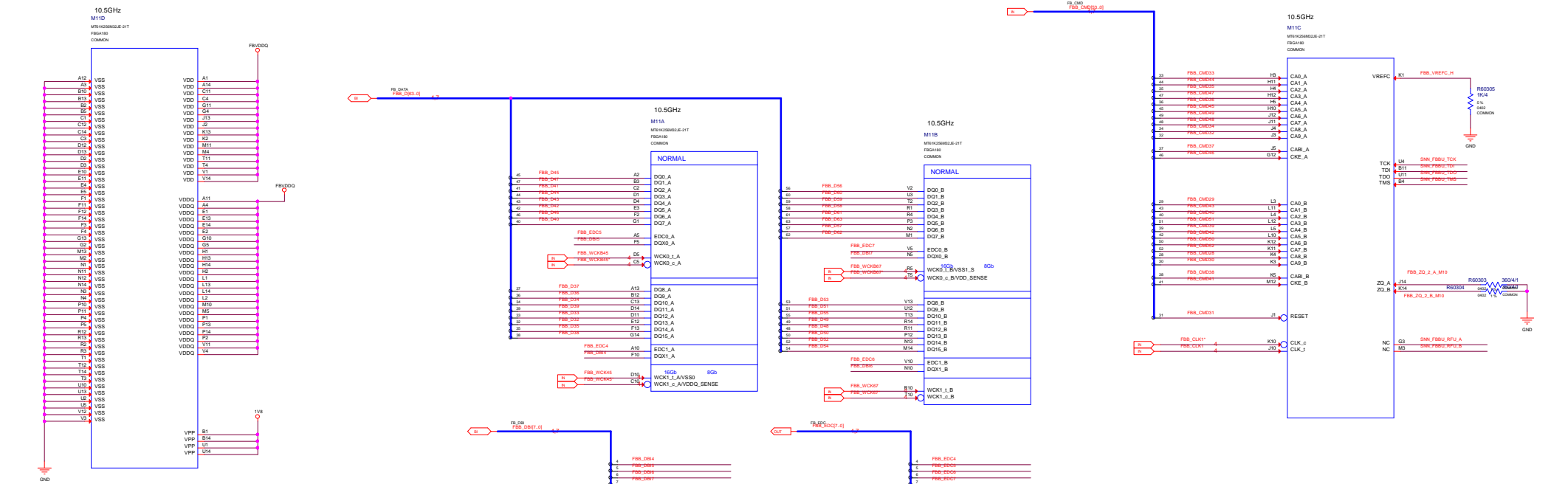
CLOSE TO DRAM: 4x 0402 1uF



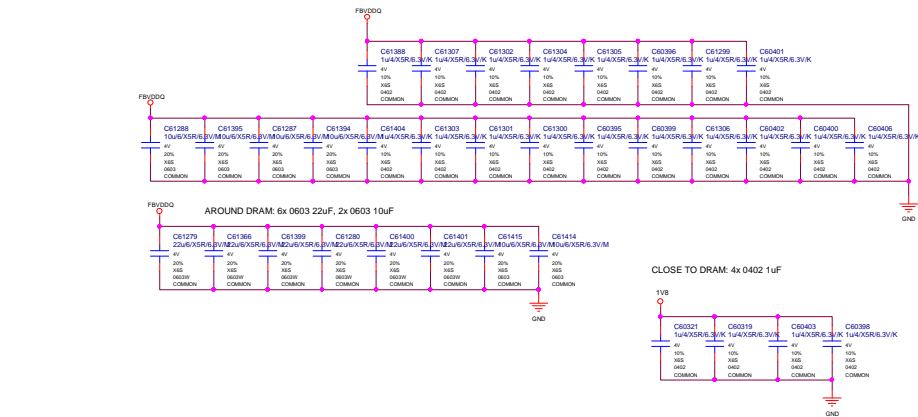
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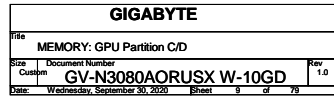
MEMORY: FBB Partition 63..32



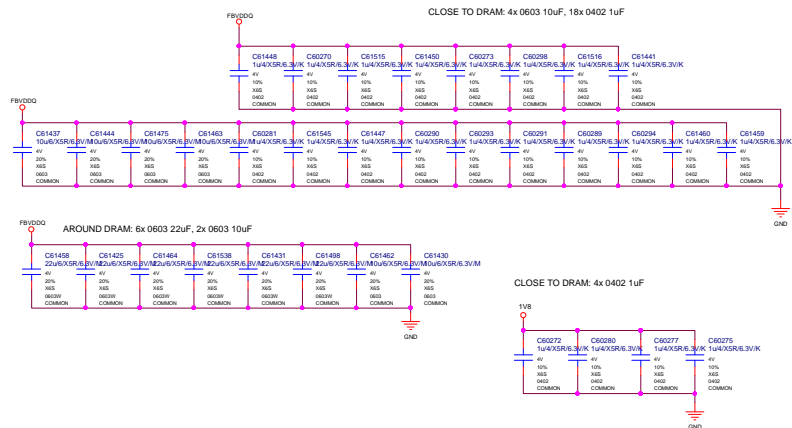
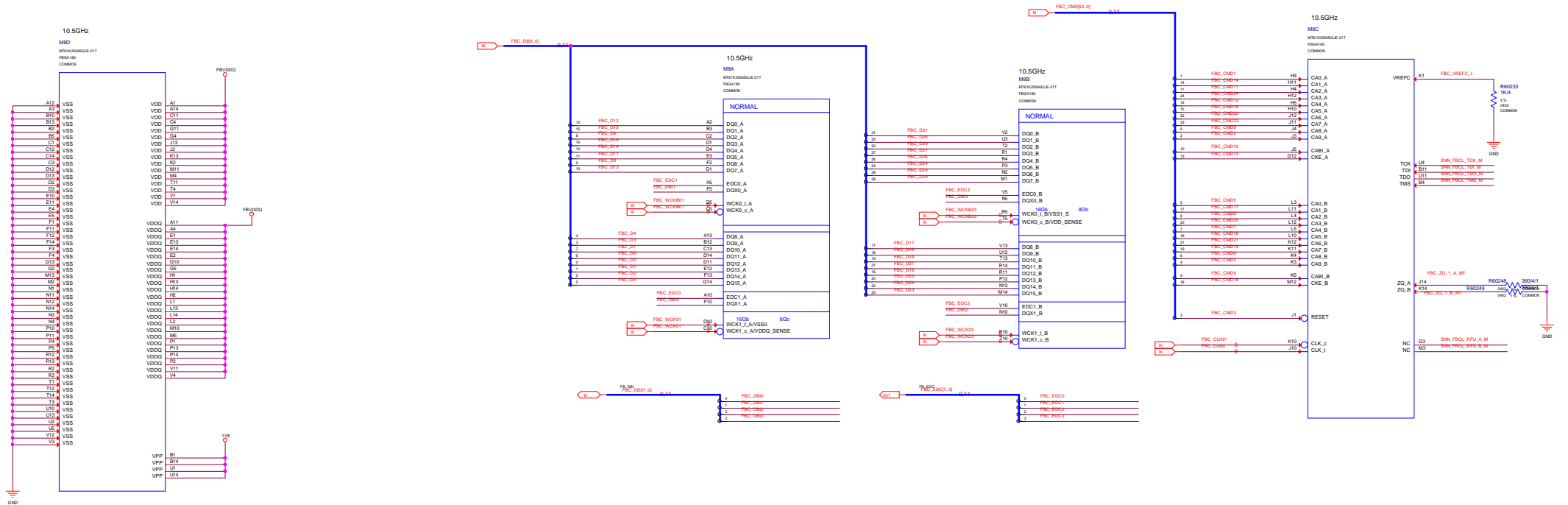
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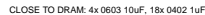
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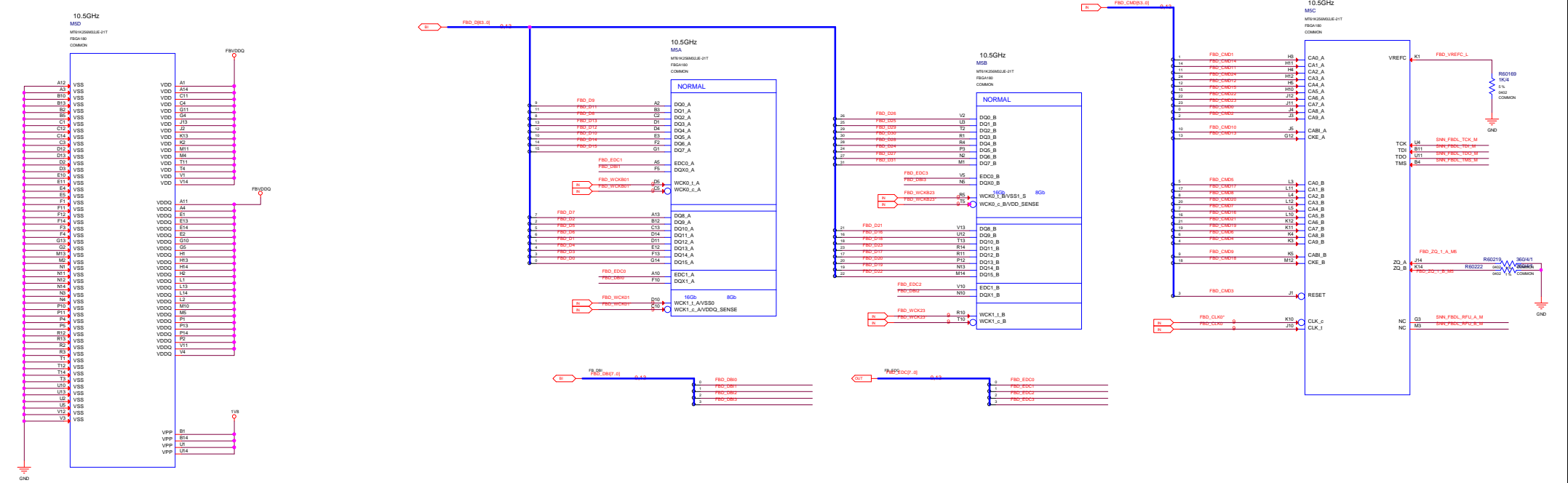
MEMORY: FBC Partition 31..0



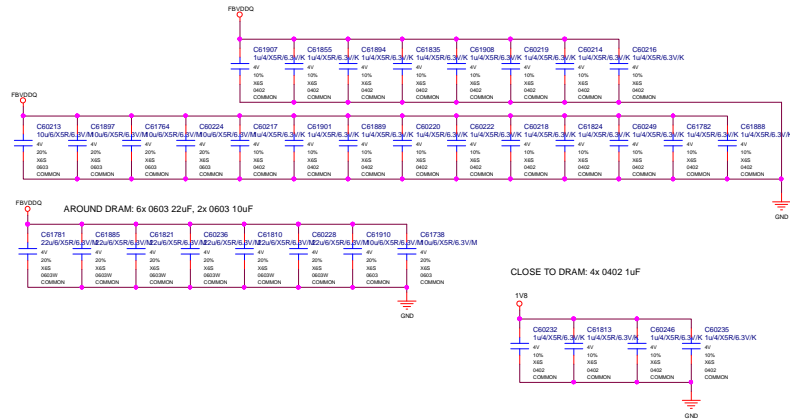
10.5GHz



MEMORY: FBD Partition 31..0

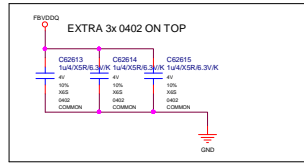
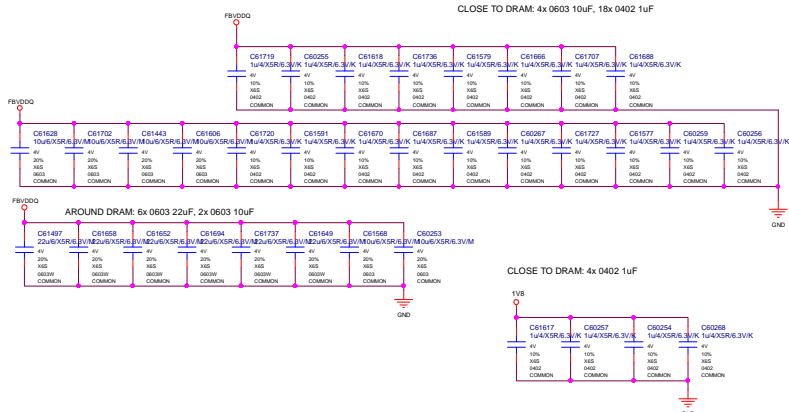
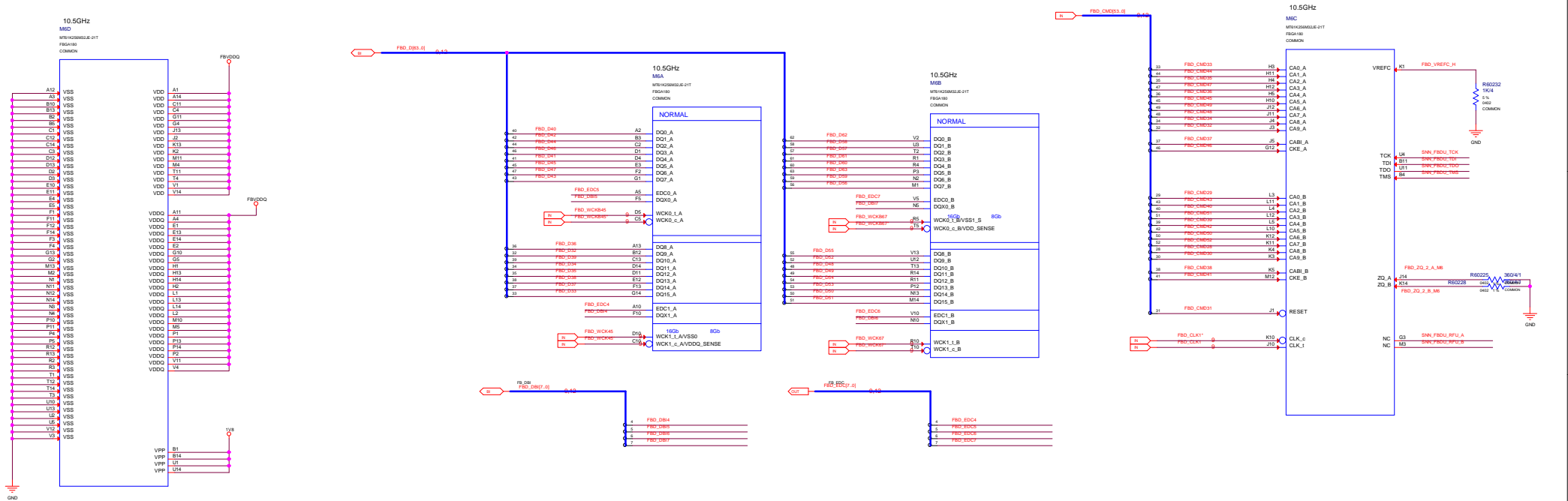


CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF

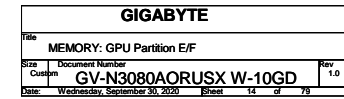


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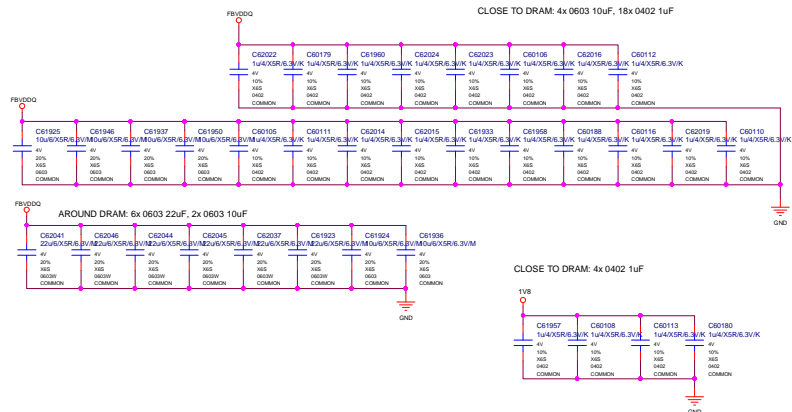
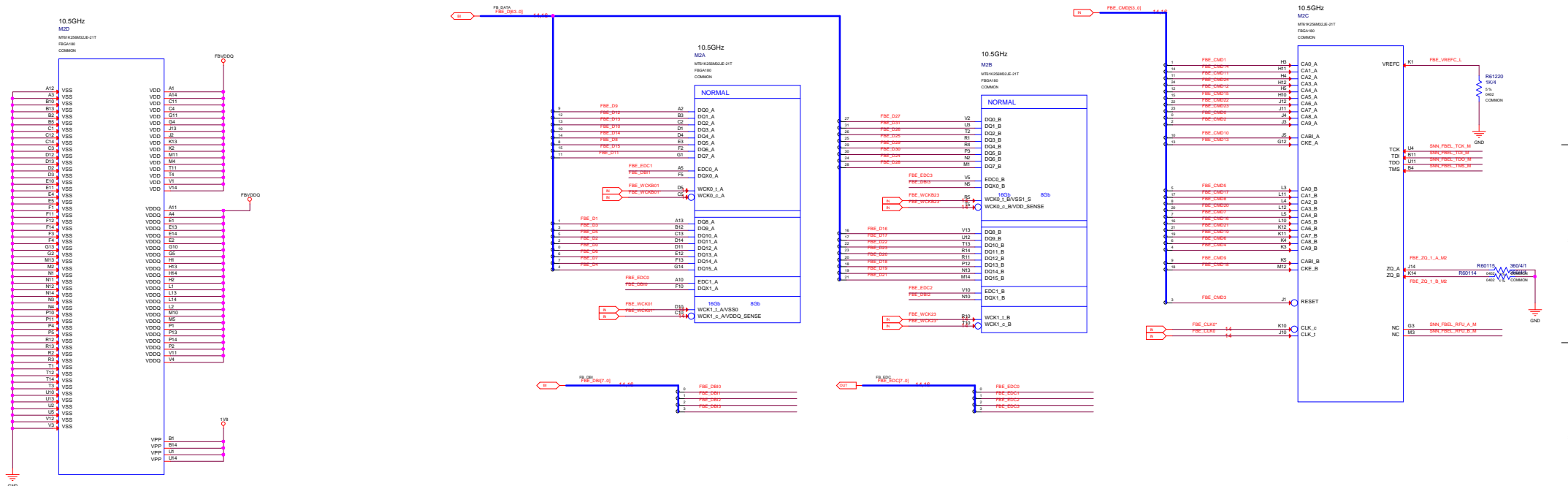
MEMORY: FBD Partition 63..32



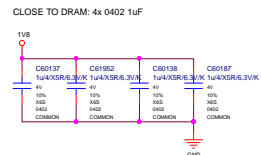
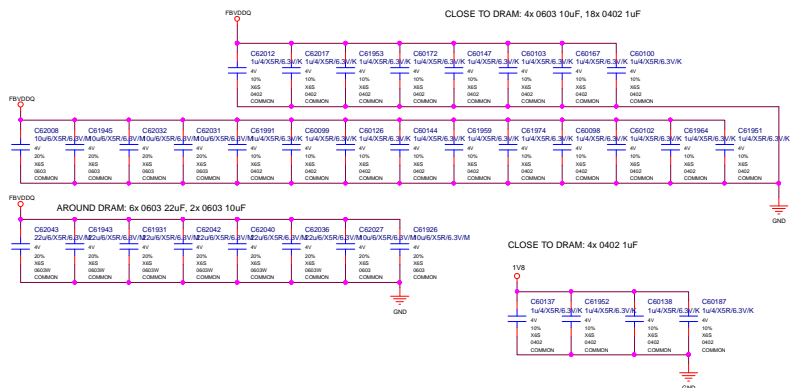
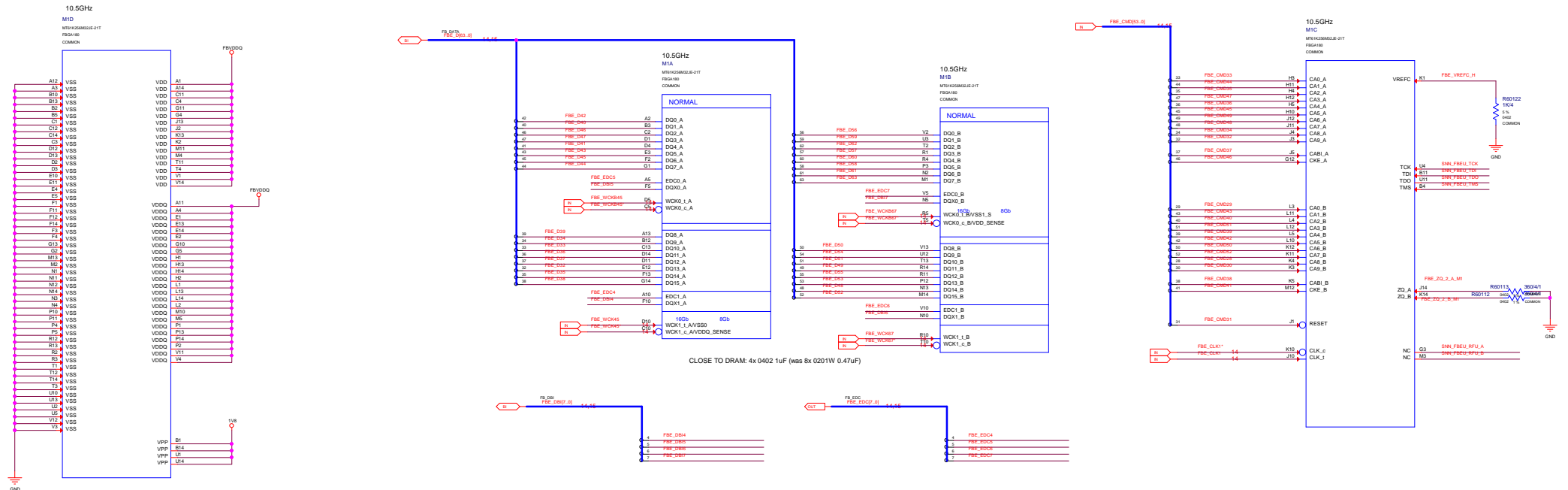
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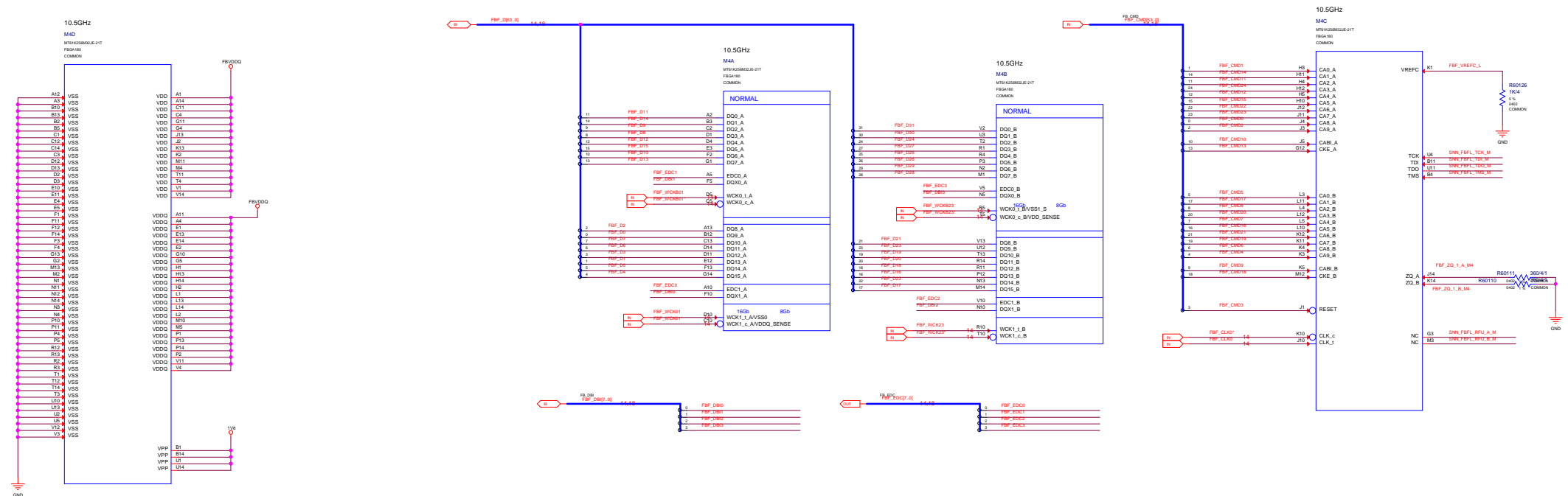
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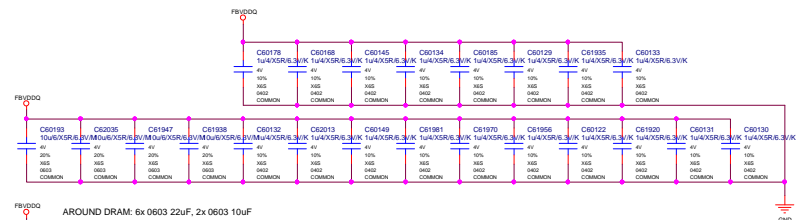
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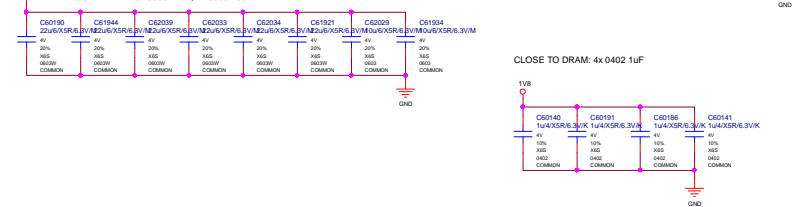
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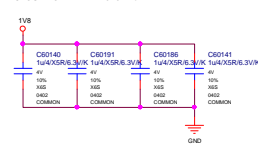
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



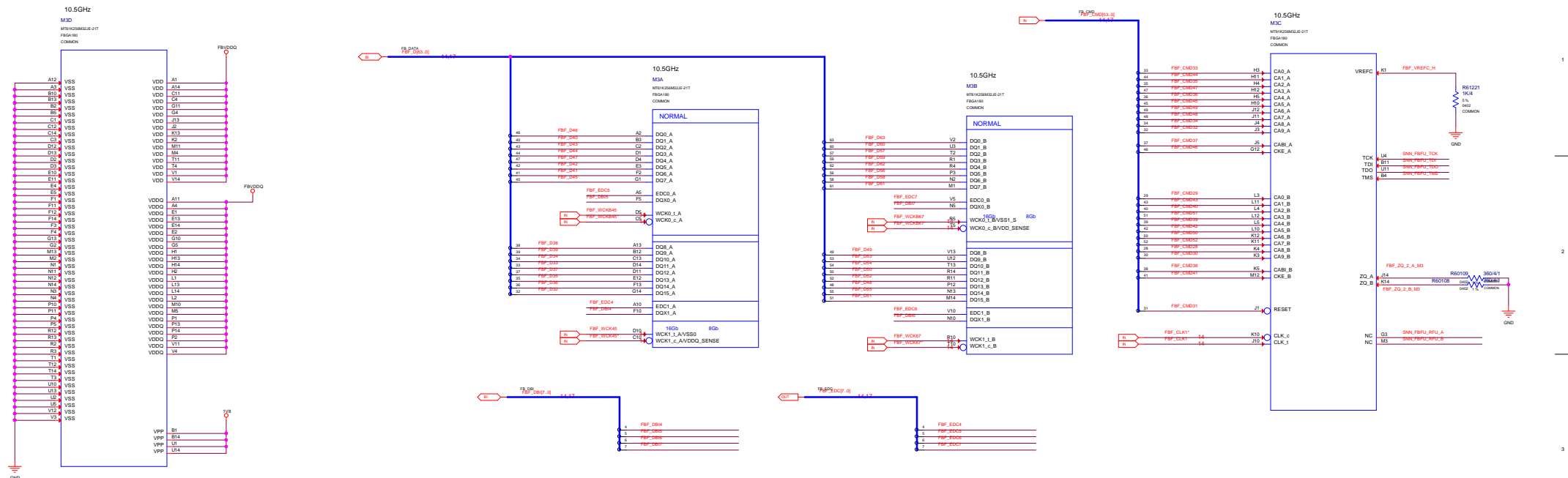
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF



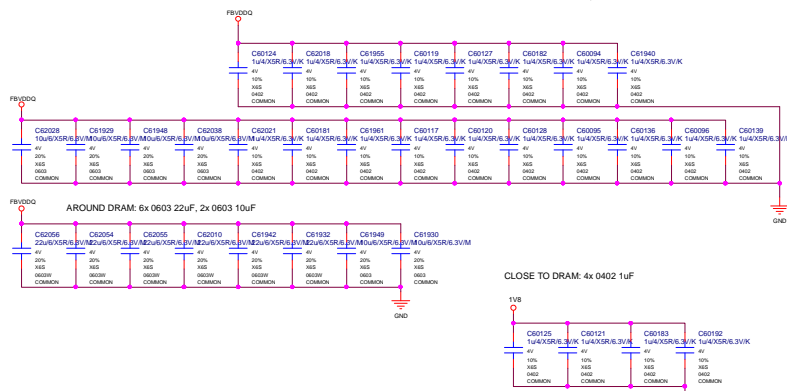
CLOSE TO DRAM: 4x 0402 1uF



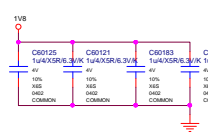
MEMORY: FBF Partition 63..32



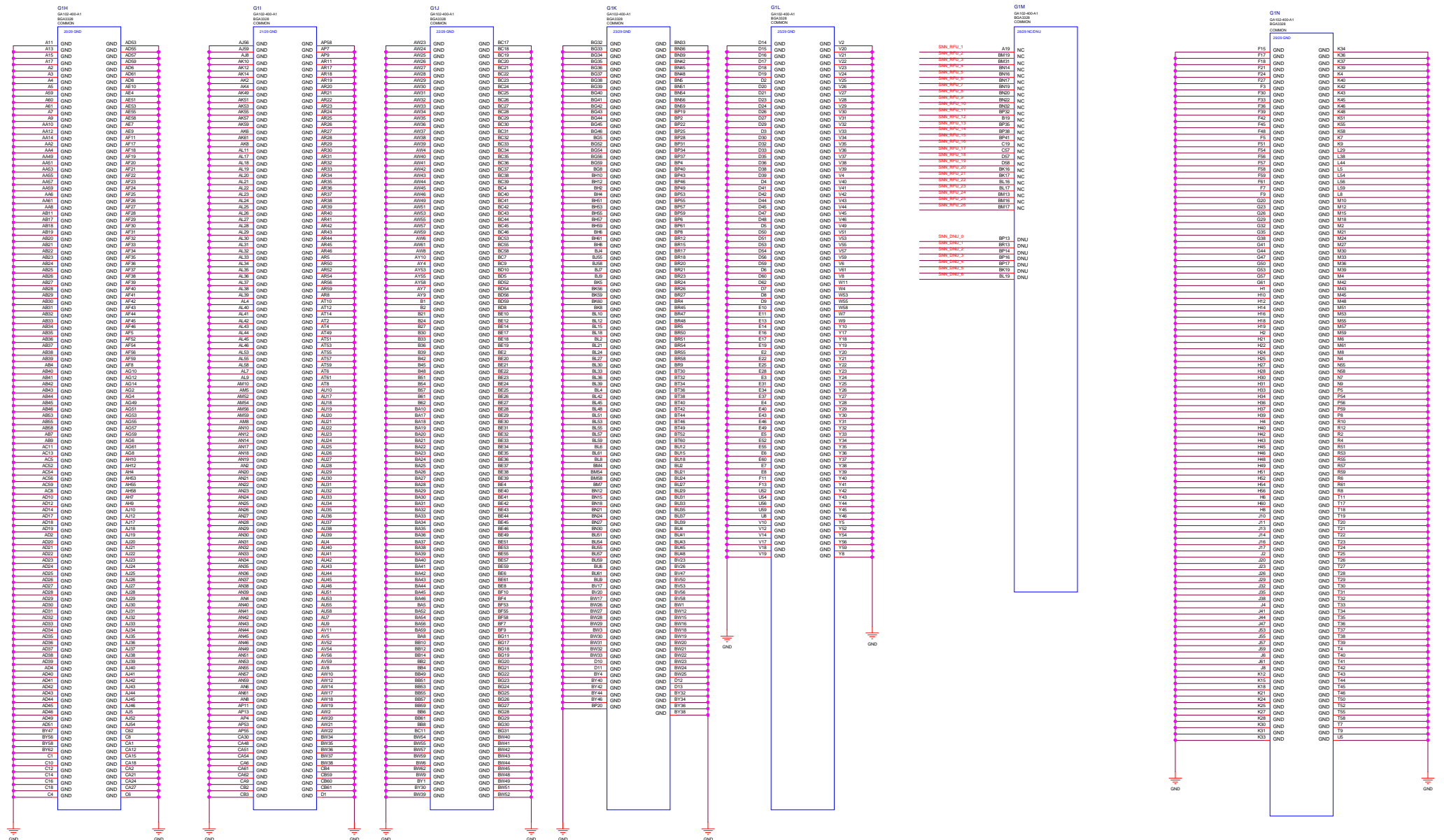
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF



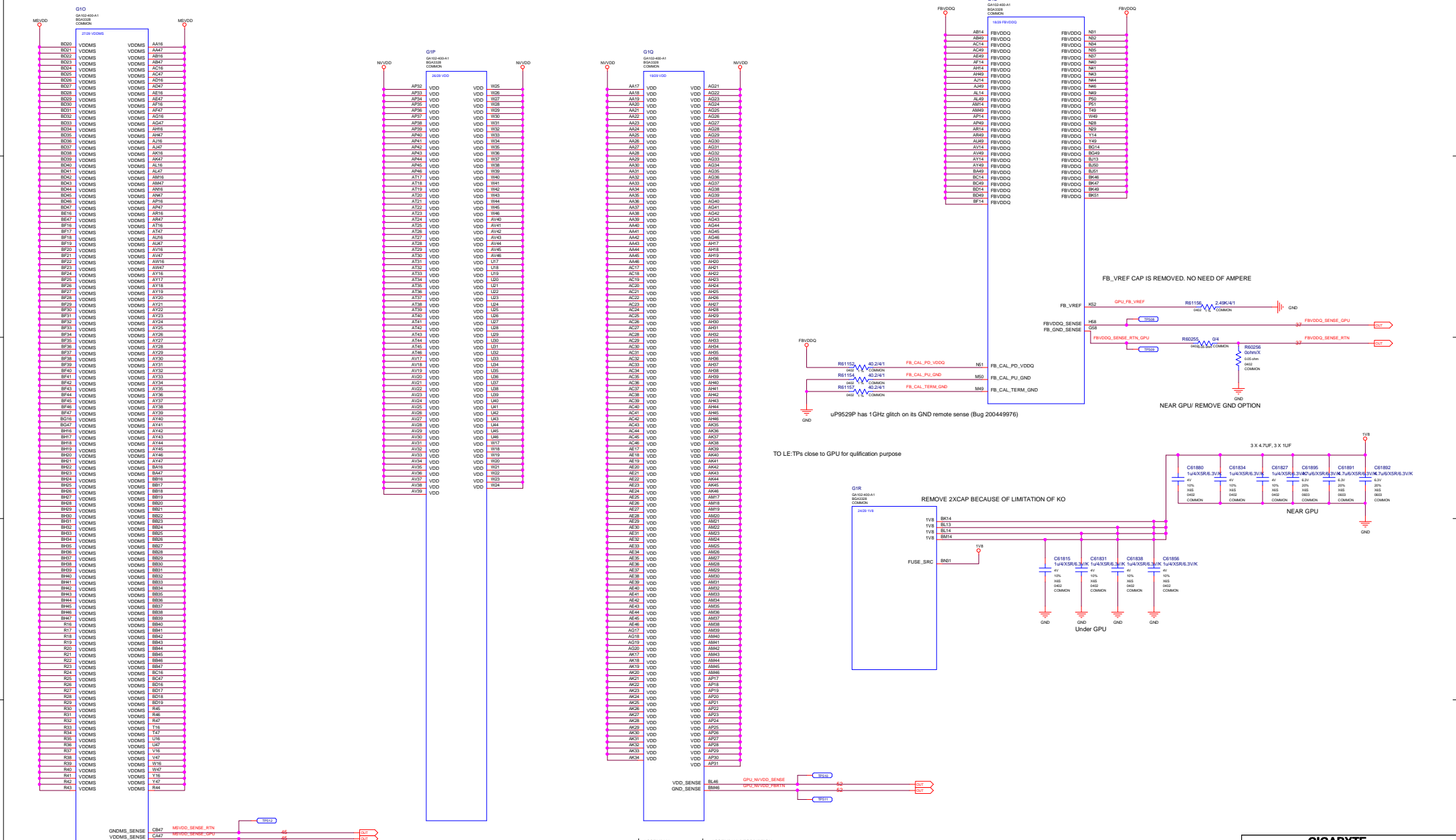
CLOSE TO DRAM: 4x 0402 1uF



GPU GND, RFUs & RSVD



GPU PWR and GND

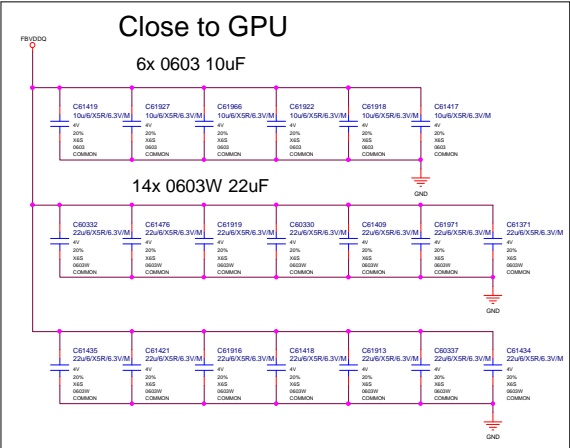
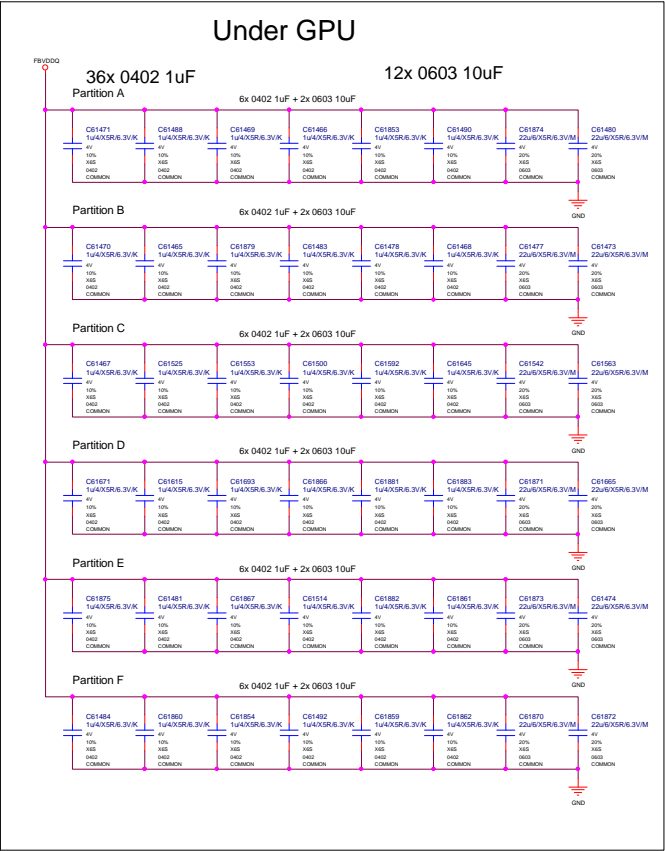


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NVVDD UNDER GPU

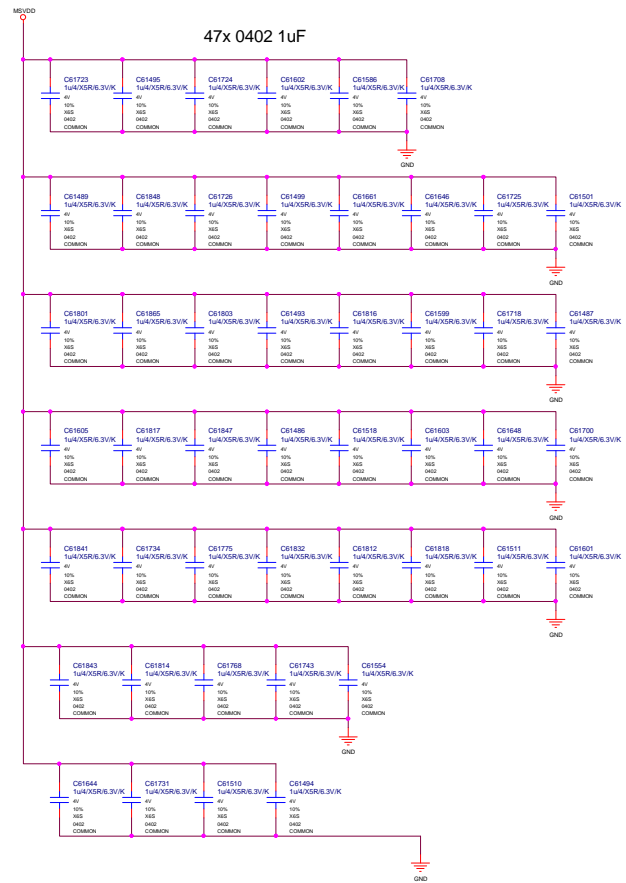
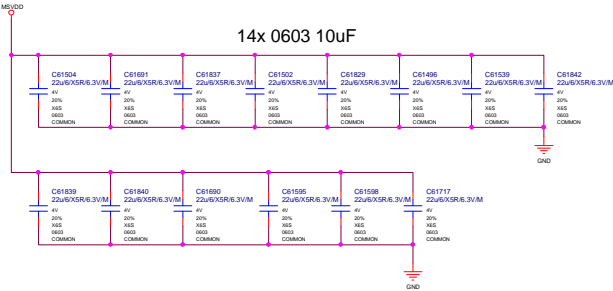


FBVDDQ

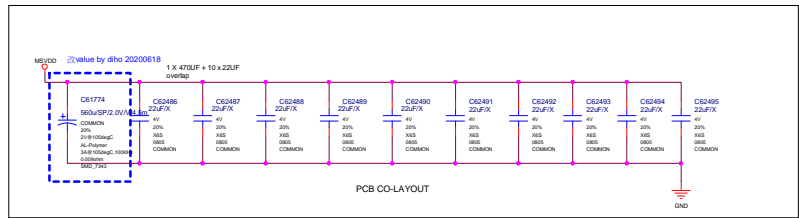
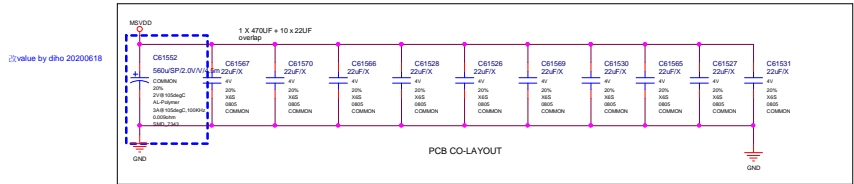


MSVDD

UNDER GPU

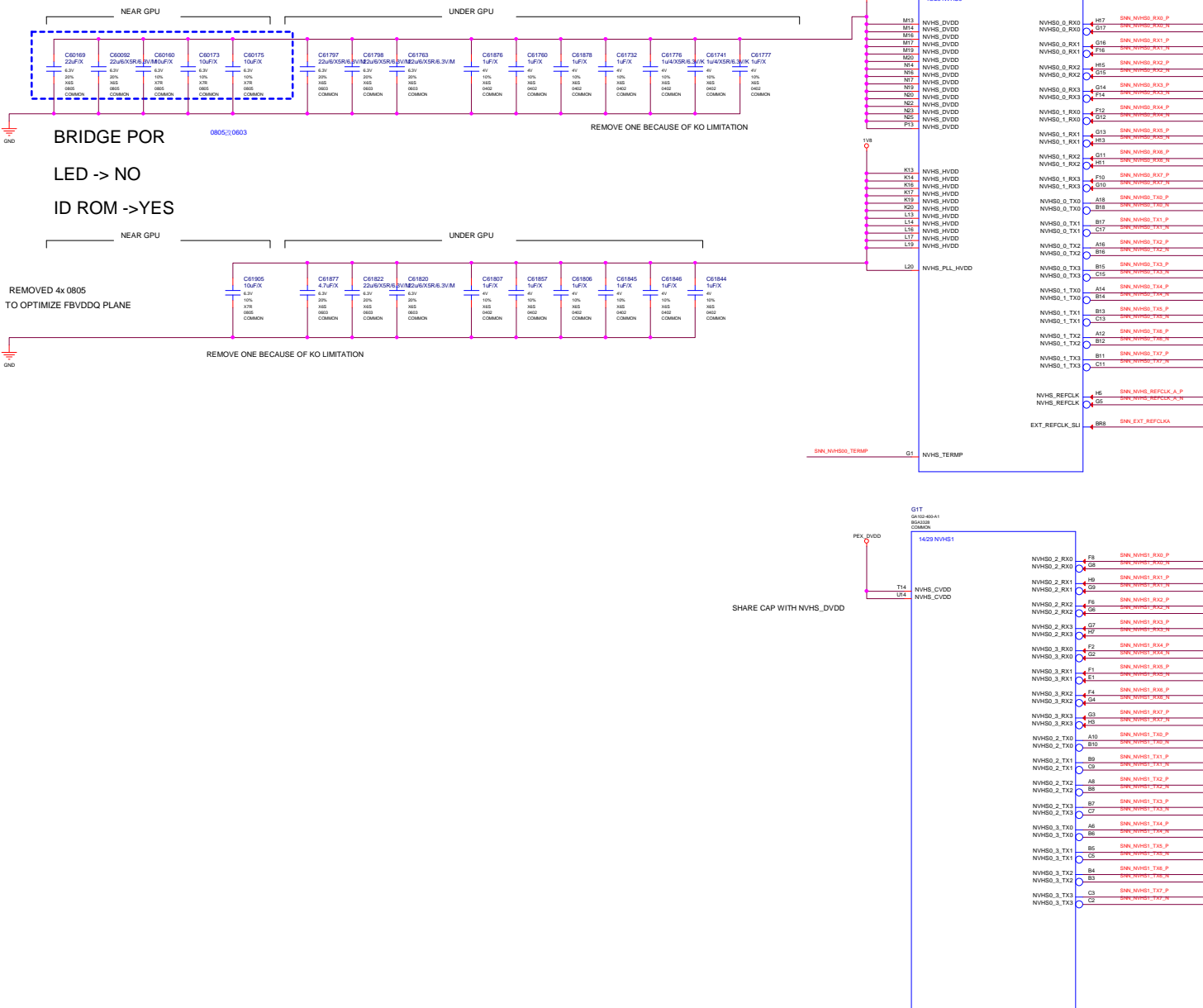


2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)

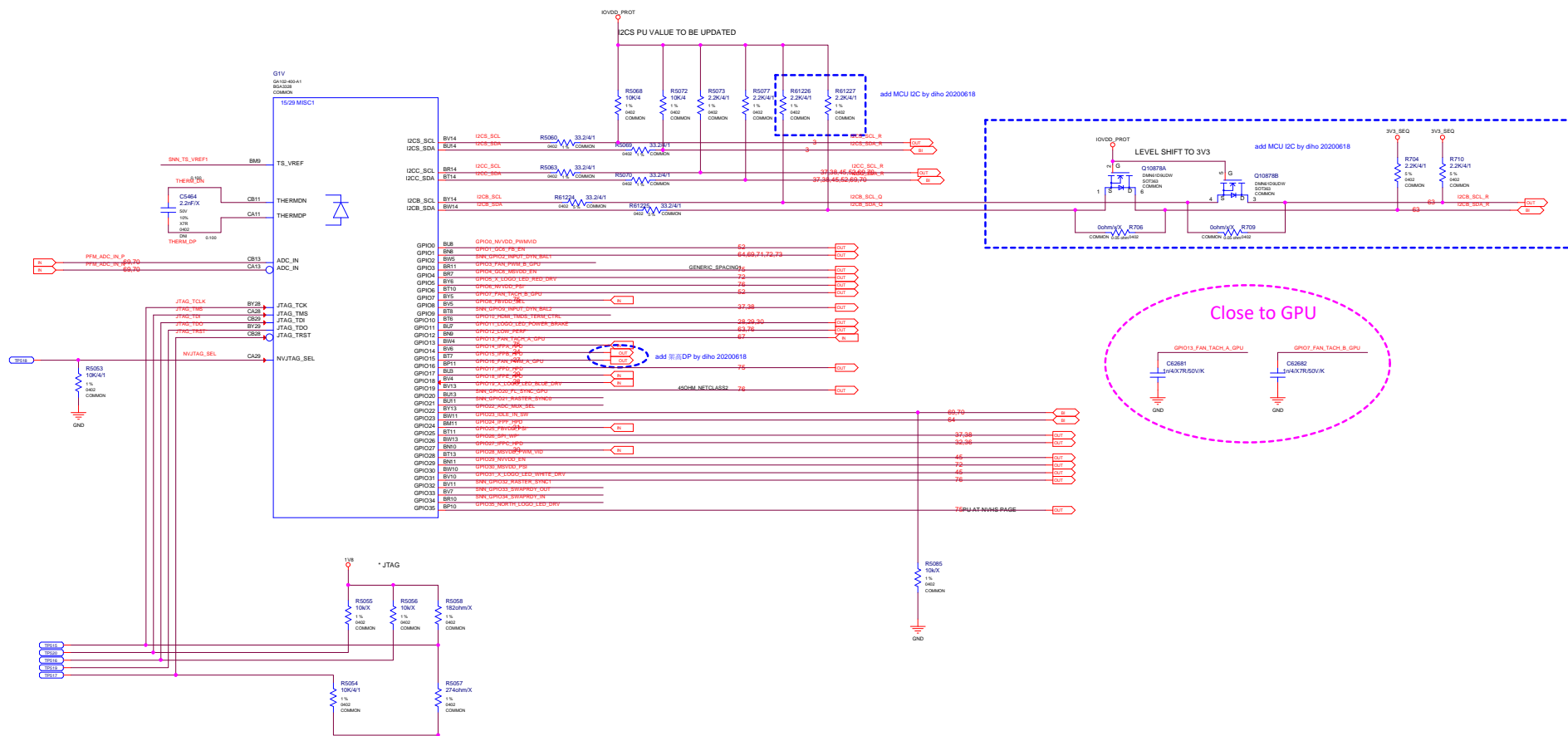


REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

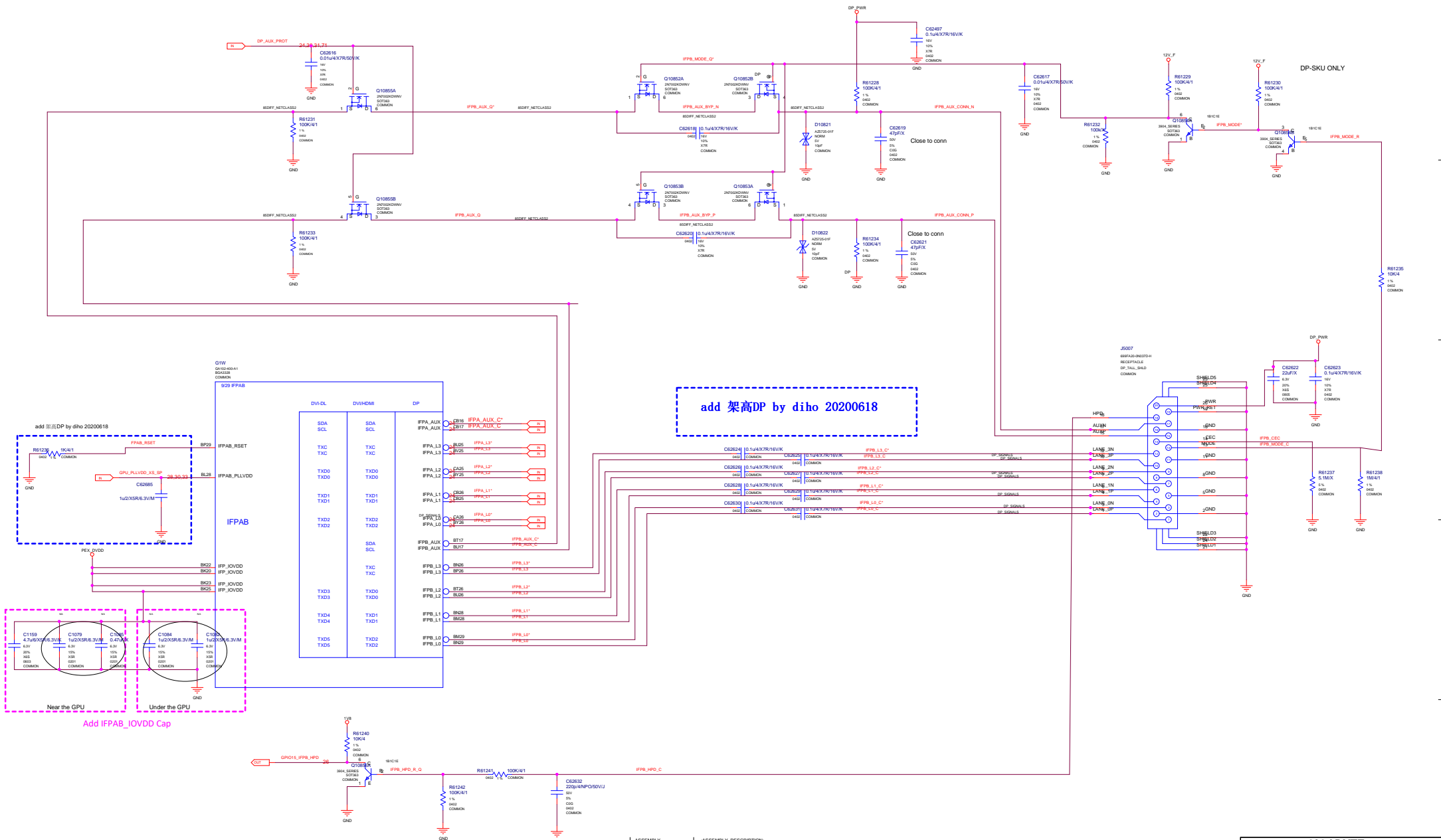
NVHS Interface and FRAME LOCK

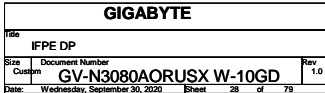


MISC1: Fan, Thermal, JTAG, GPIO, STEREO

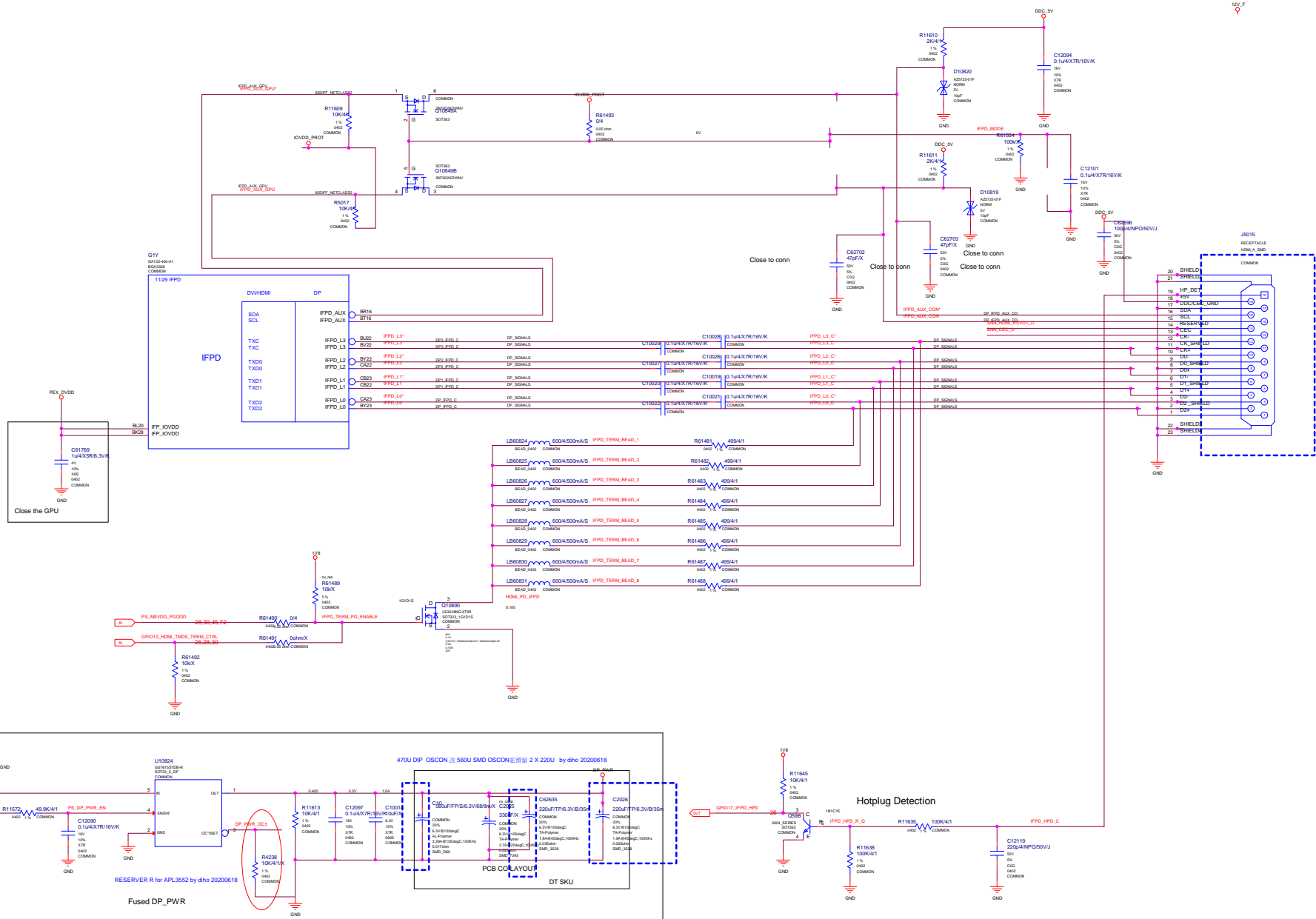


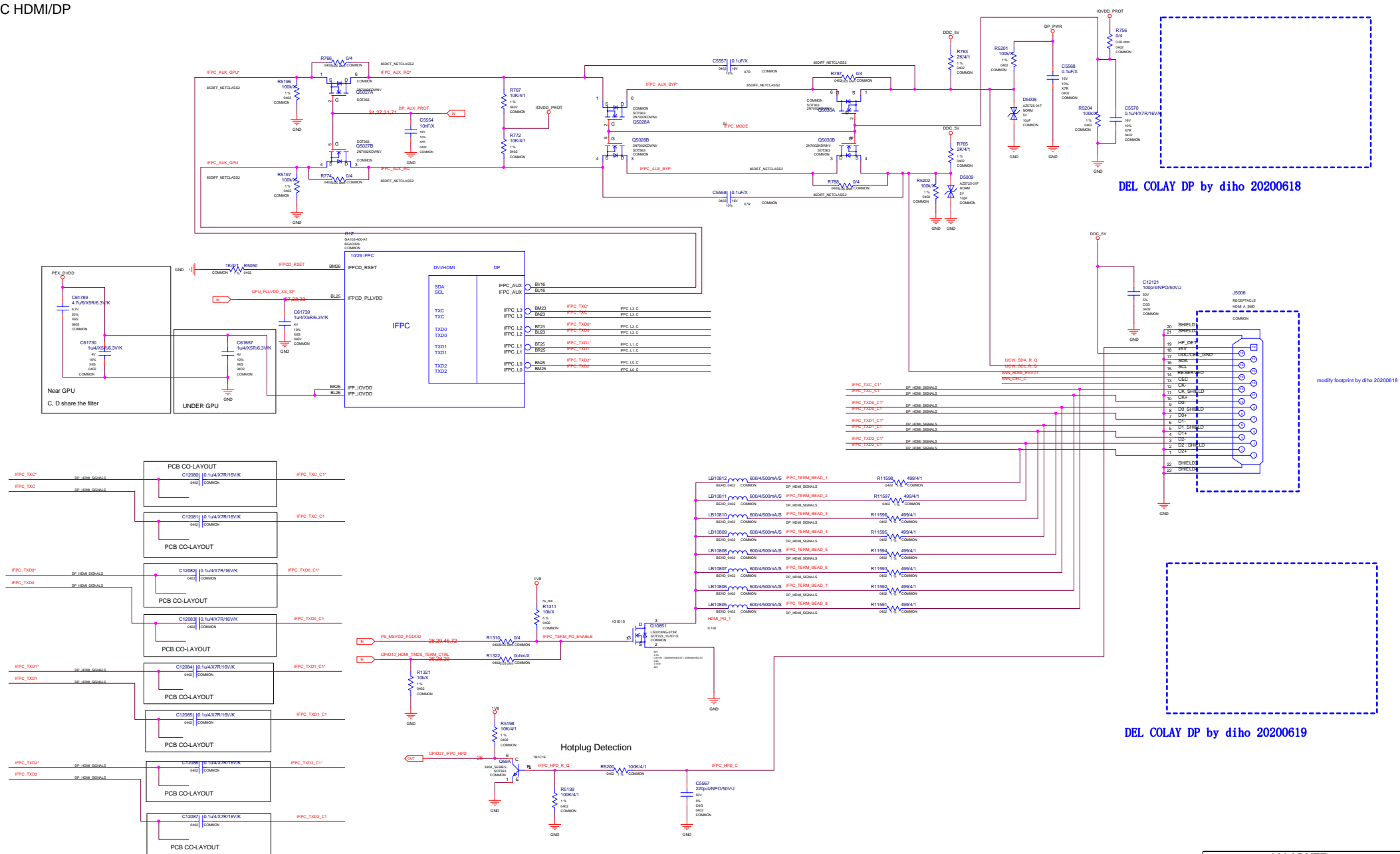
IFPA UNUSED, IFPB UNUSED

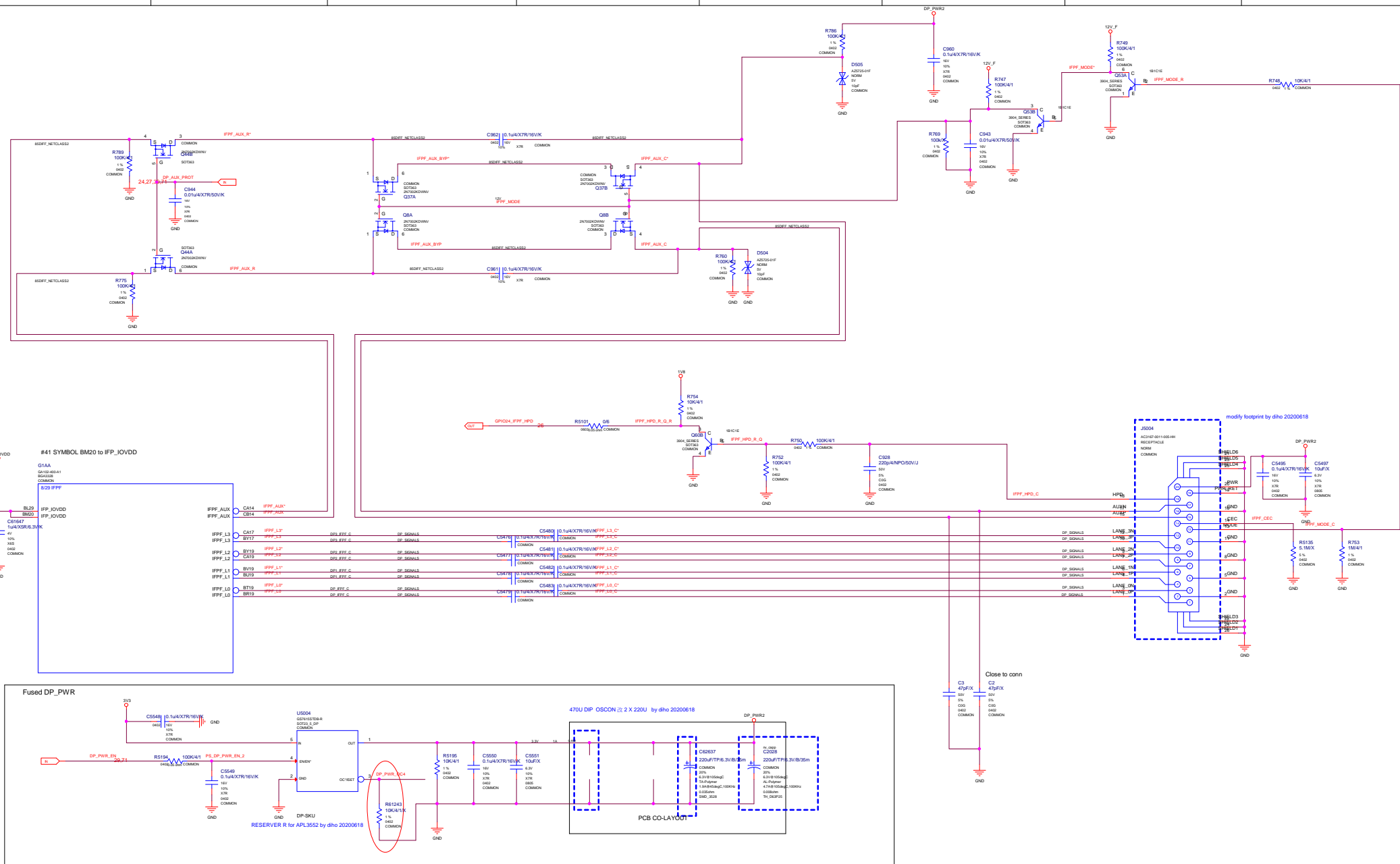




IFPD DP







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MISC: ROM, Straps

GROUP0 STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0].FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

DEFAULT

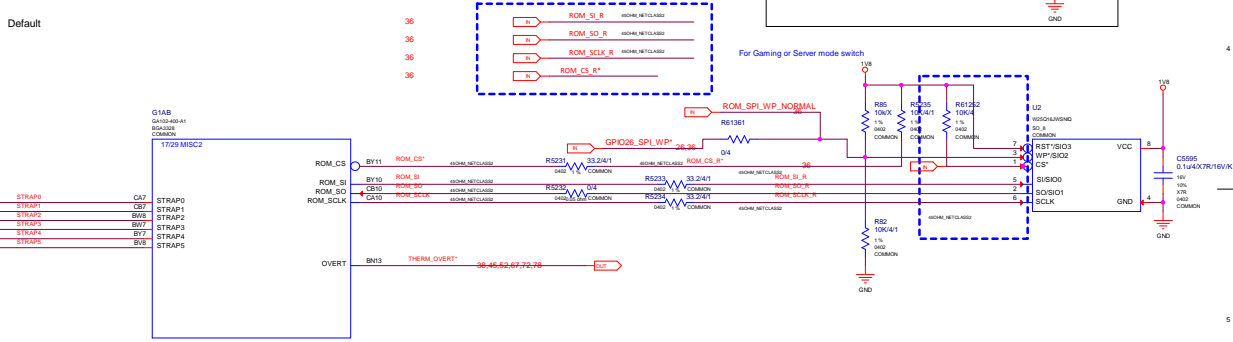
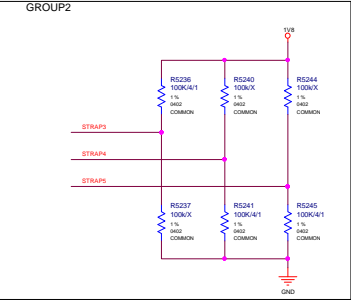
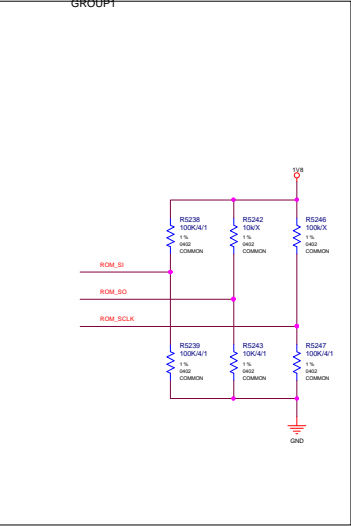
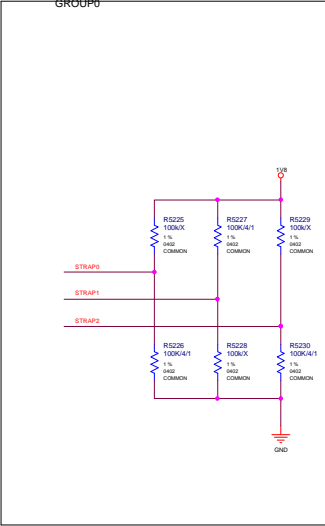
Default

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

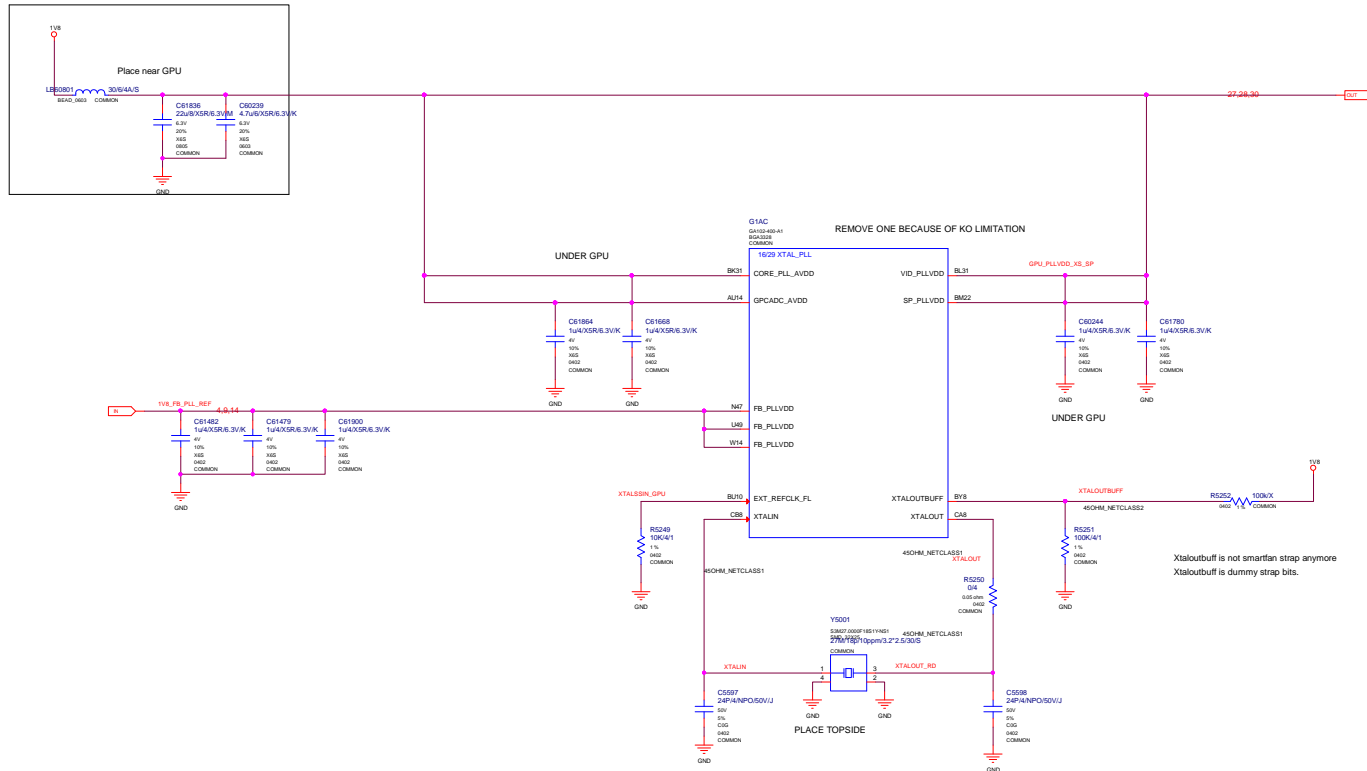
<-A01 PCB

<-OLD

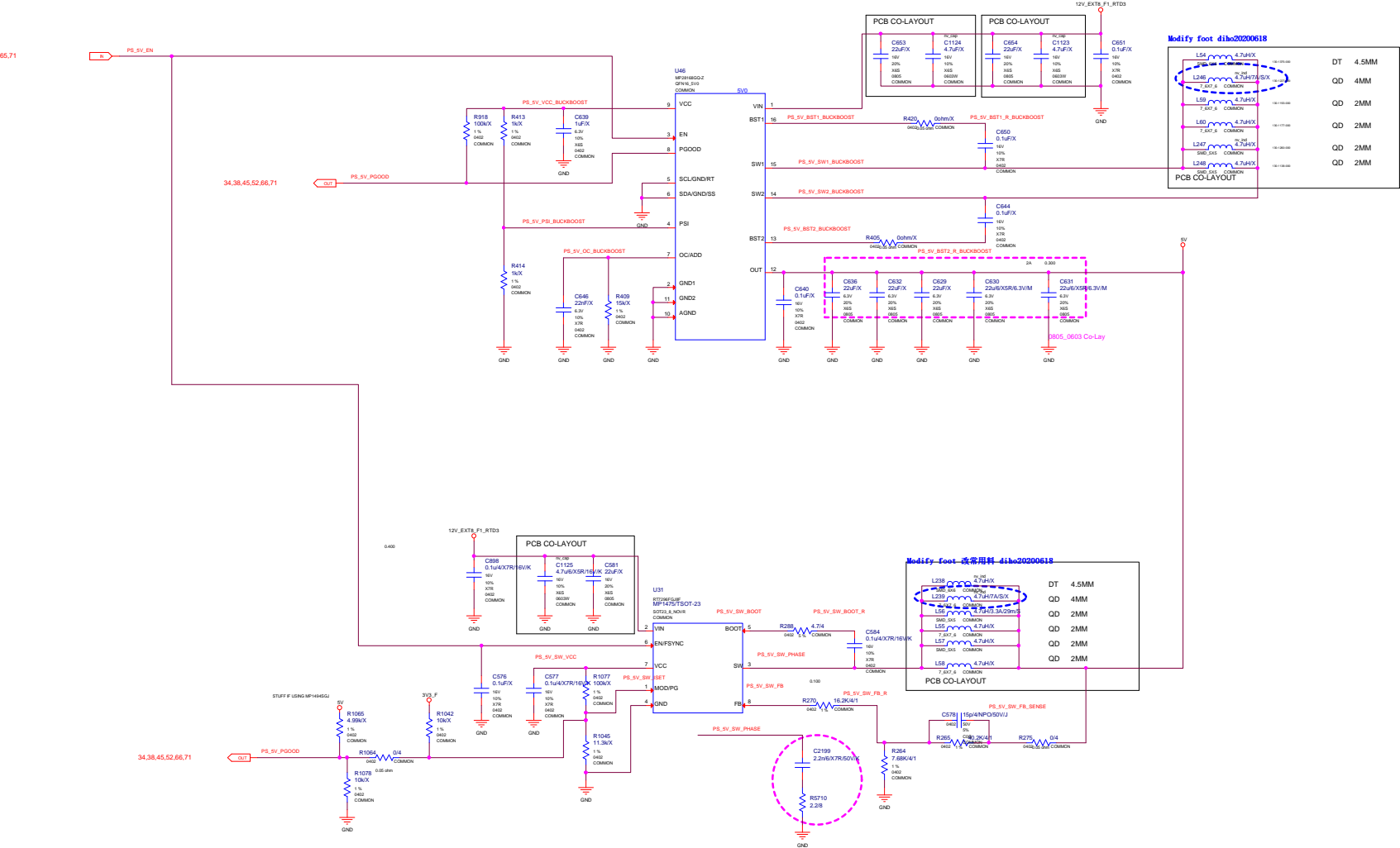
<-LATEST A02 PCB



MISC: XTAL. PLL

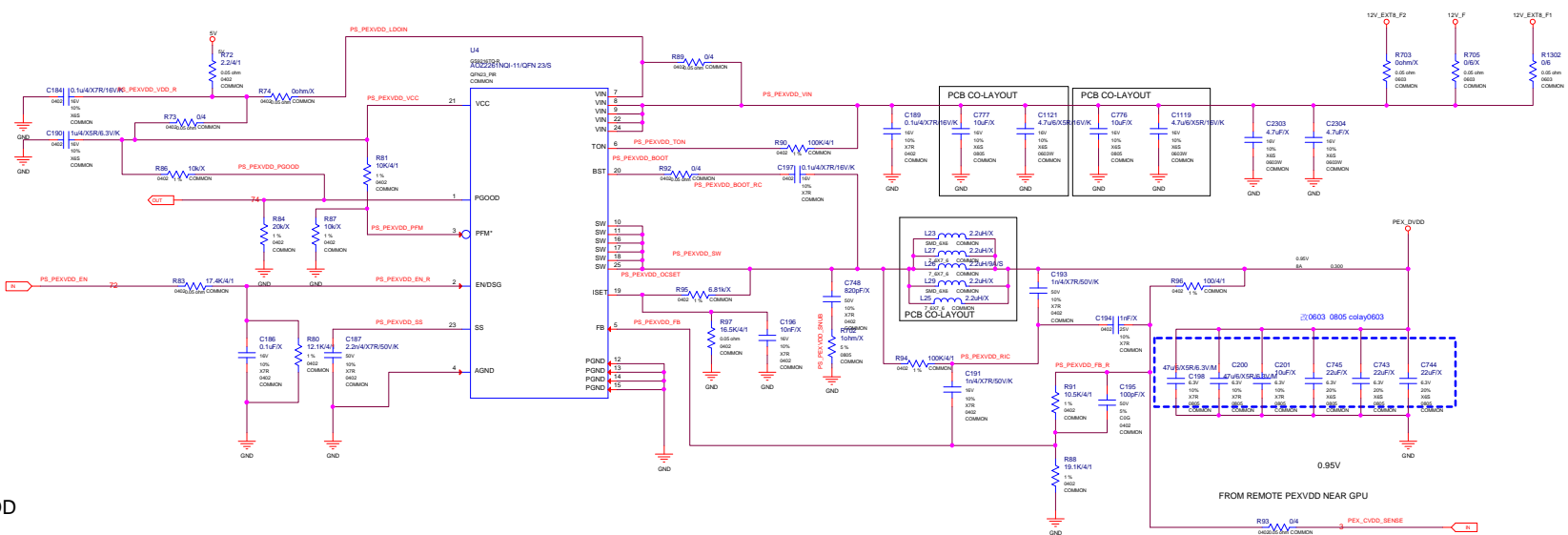


PS: 5V, 5V_BACKUP

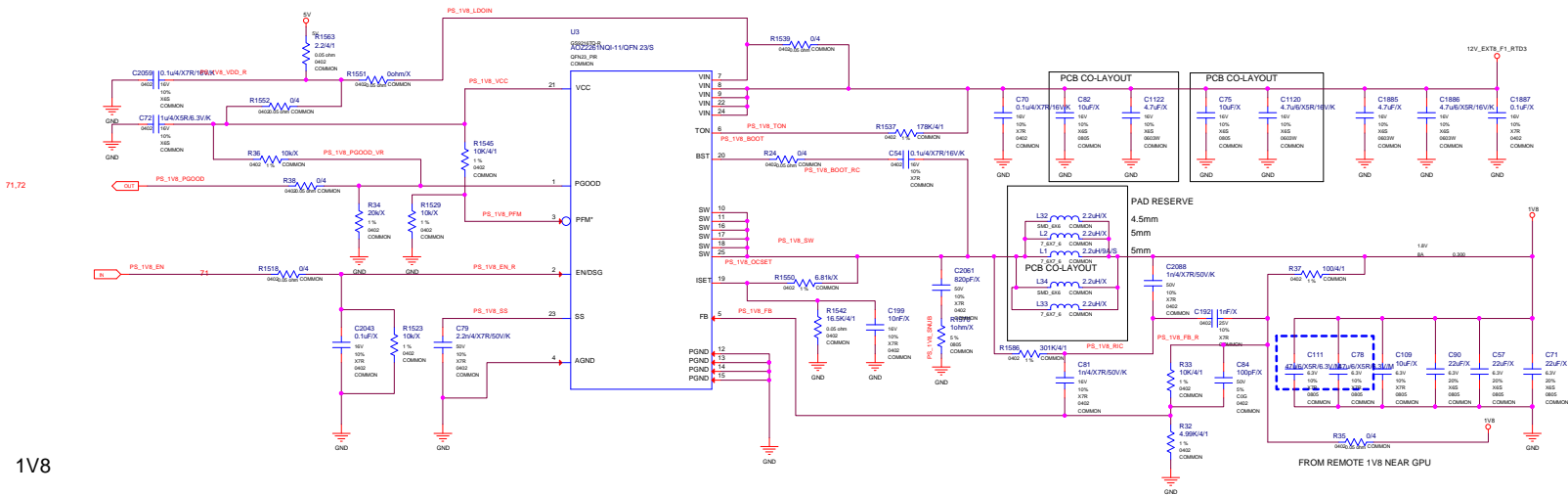


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ASSEMBLY PAGE DETAIL
-ASSEMBLY DESCRIPTION-
PS: 5V



PEX_DVDD



1V8

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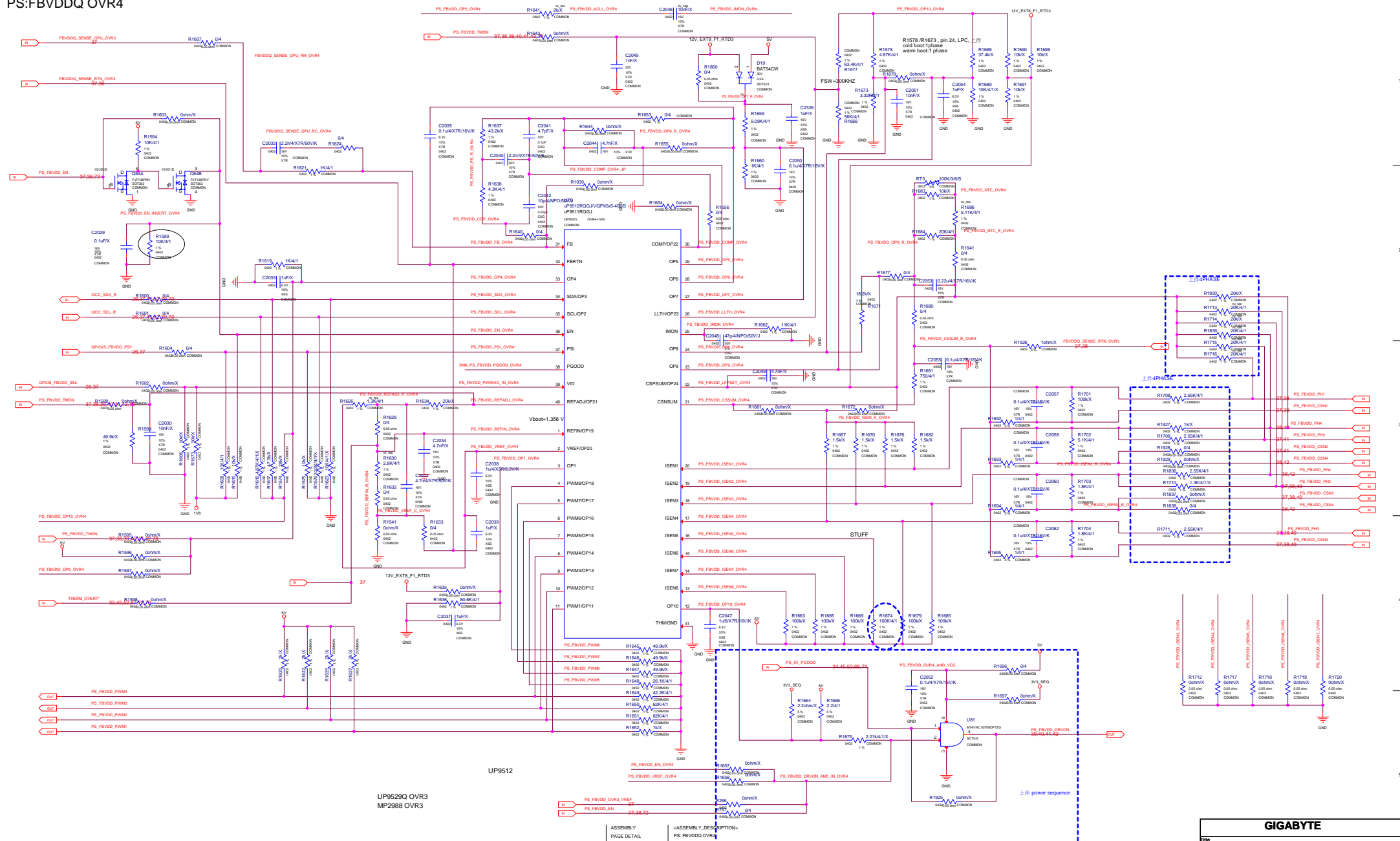
ASSEMBLY
PAGE DETAIL

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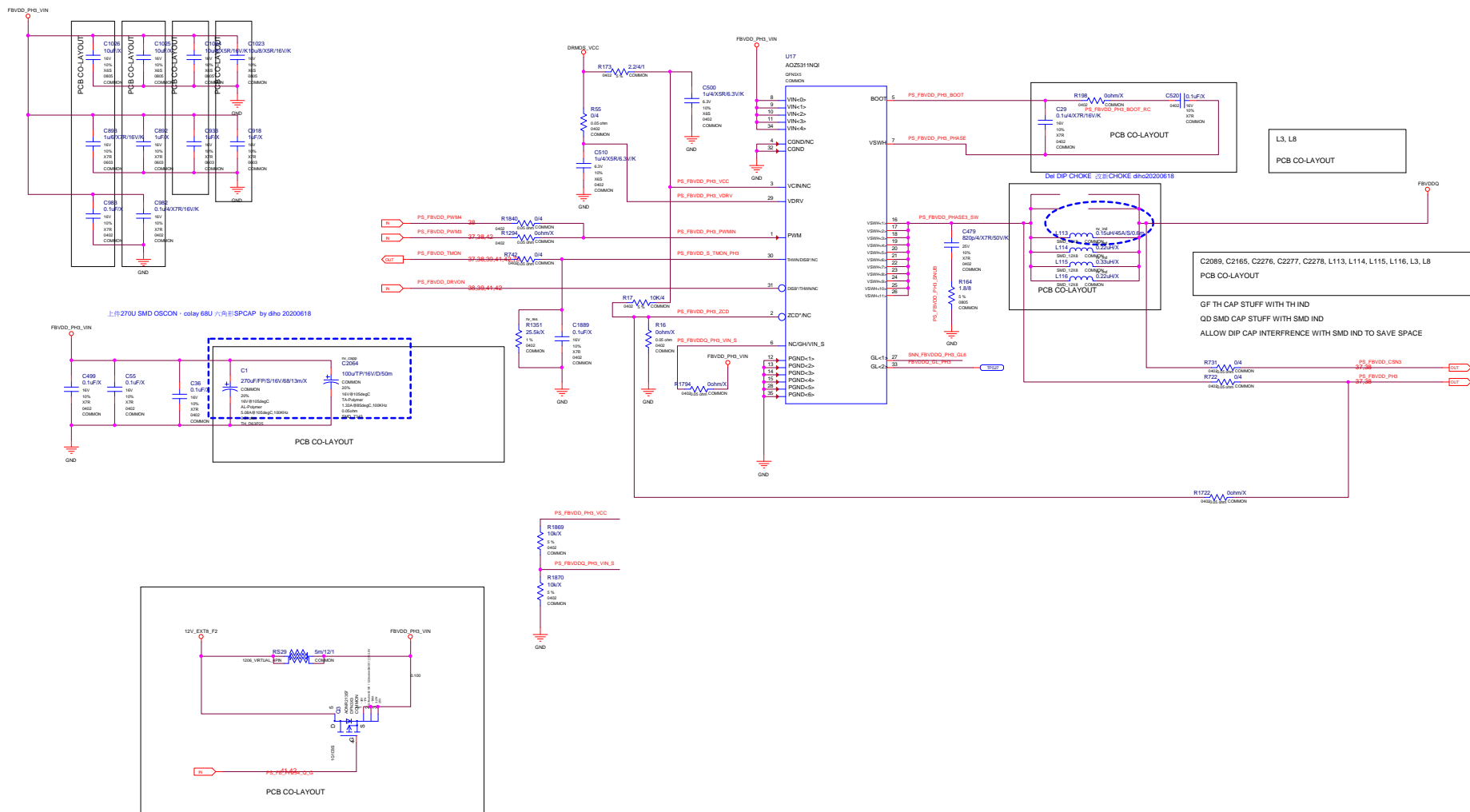
FOR DT SKU



PS:FBVDDQ OVR4



PS: FBVDD PH3

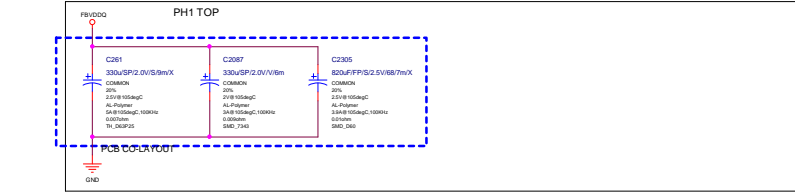


FBVDD PH3 INPUT ANTI-BACKDRIVE

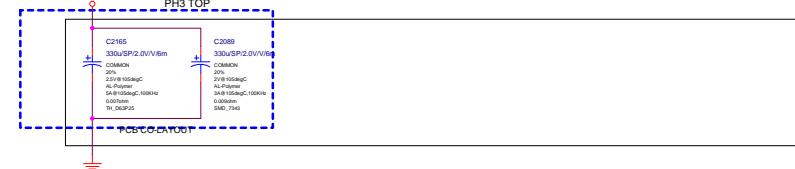
PS: FBVDD OUTPUT CAP

3x 820uF TH FBVDD OUTPUT BULK CAPS

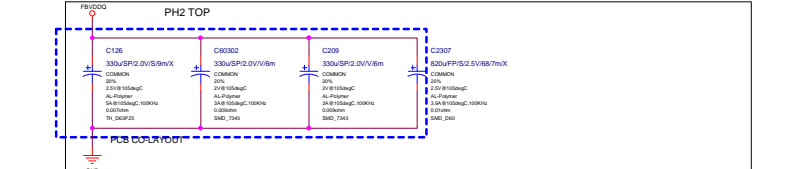
820U DIP OSCON 3300U 前置在 BOT - 原SMD OSCON改寄用kootprint上件820U by dho 20200619



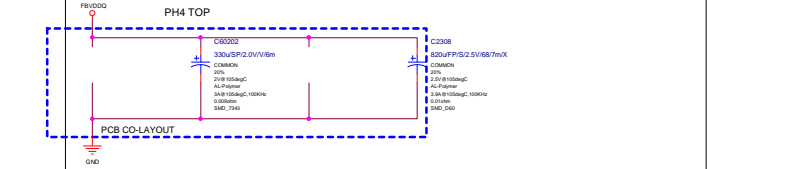
820U DIP OSCON 3300U SMD 7343 by dho 20200619



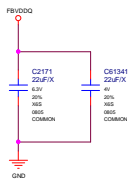
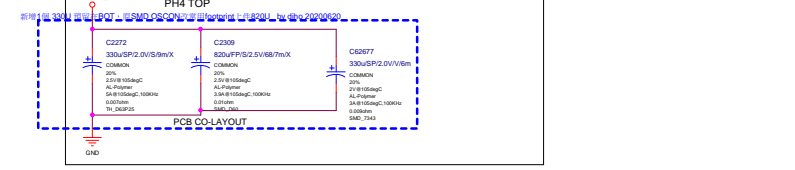
820U DIP OSCON 3300U 前置在 BOT - 原SMD OSCON改寄用kootprint上件820U by dho 20200619



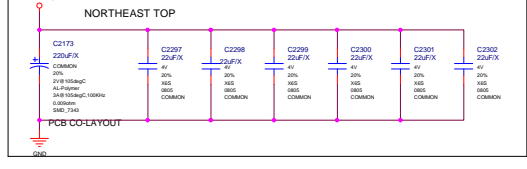
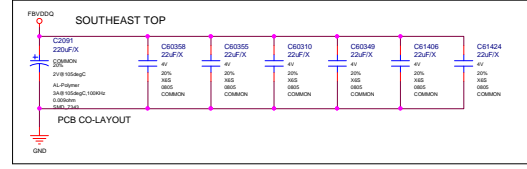
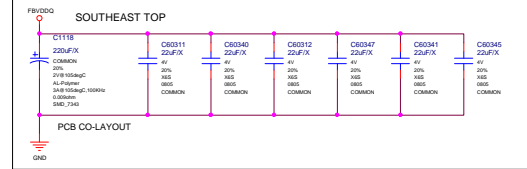
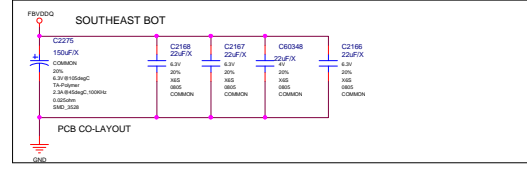
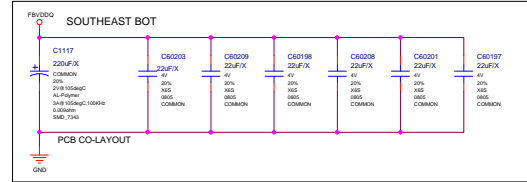
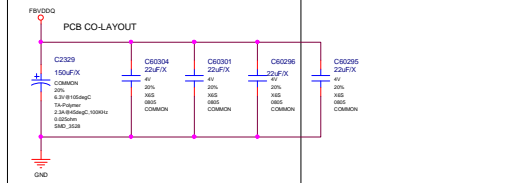
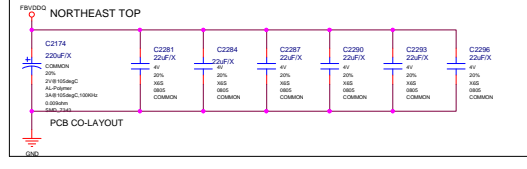
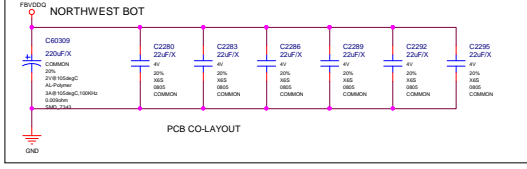
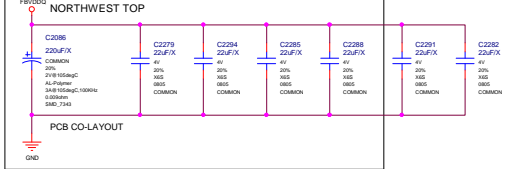
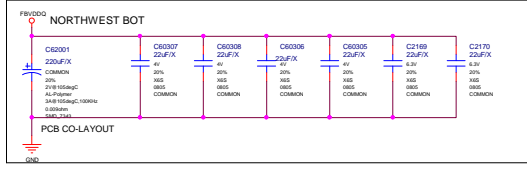
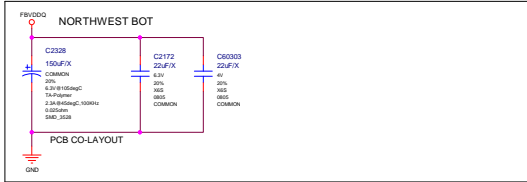
820U DIP OSCON 3300U 前置在 BOT - 原SMD OSCON改寄用kootprint上件820U by dho 20200619



前置在 BOT - 原SMD OSCON改寄用kootprint上件820U by dho 20200620



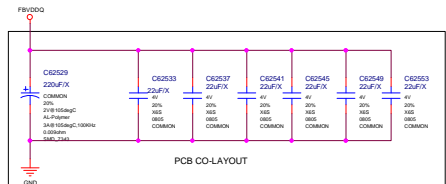
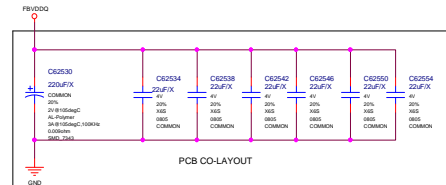
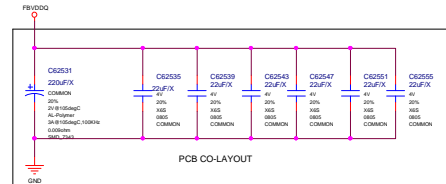
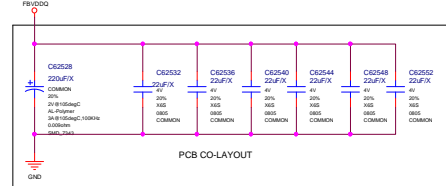
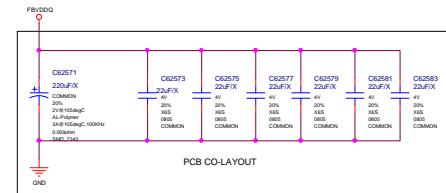
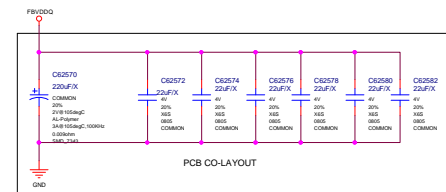
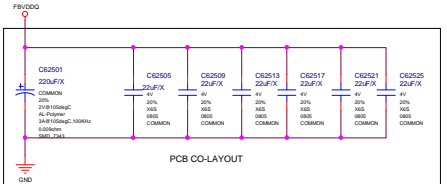
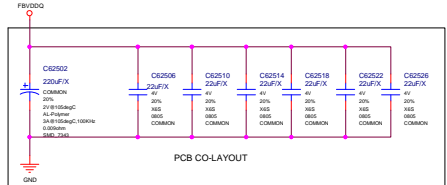
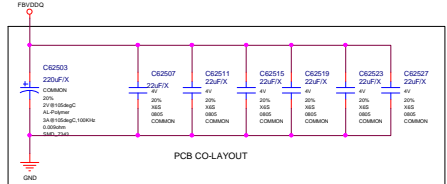
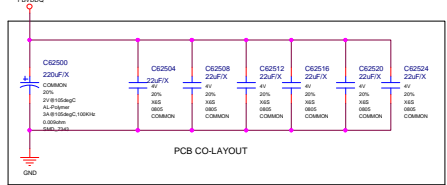
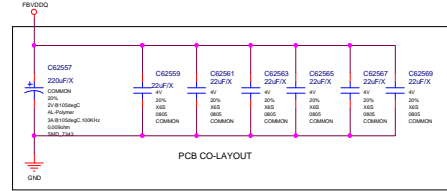
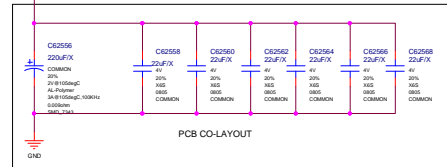
CLOSE TO FB PH3 OUTPUT STUFF



GIGABYTE

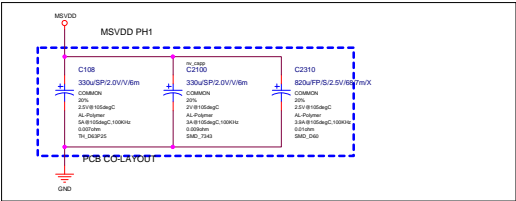
Added for A01 x16

ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES

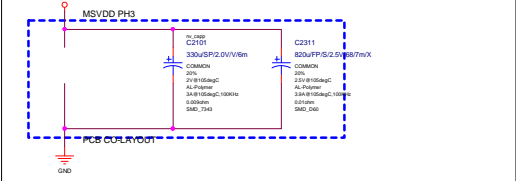


PS:MSVDD OUTPUT CAP (TOP)

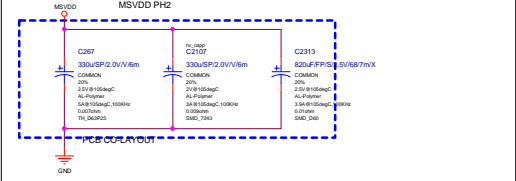
820U DIP OSCON 330U 預留在BOT，需SMD OSCON改常用footprint上件820U by dho 20200619



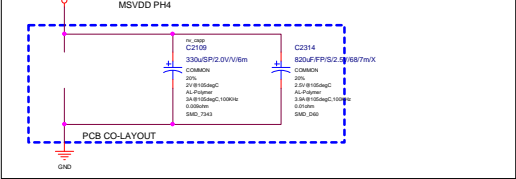
820U DIP OSCON 330U 預留在BOT，需SMD OSCON改常用footprint上件820U by dho 20200619



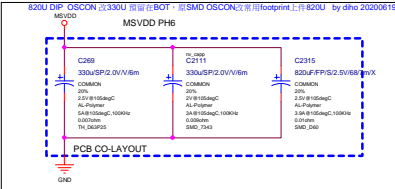
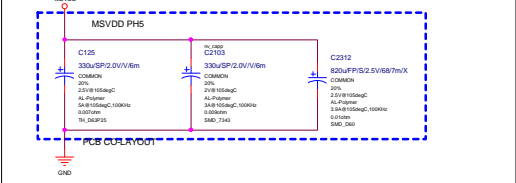
820U DIP OSCON 330U 預留在BOT，需SMD OSCON改常用footprint上件820U by dho 20200619



820U DIP OSCON 330U 預留在BOT，需SMD OSCON改常用footprint上件820U by dho 20200619



820U DIP OSCON 330U 預留在BOT，需SMD OSCON改常用footprint上件820U by dho 20200619



MSVDD PH6 ASIDE

	A	B	C	D	E	F	G	H
1								
2								
3								
4								
5								

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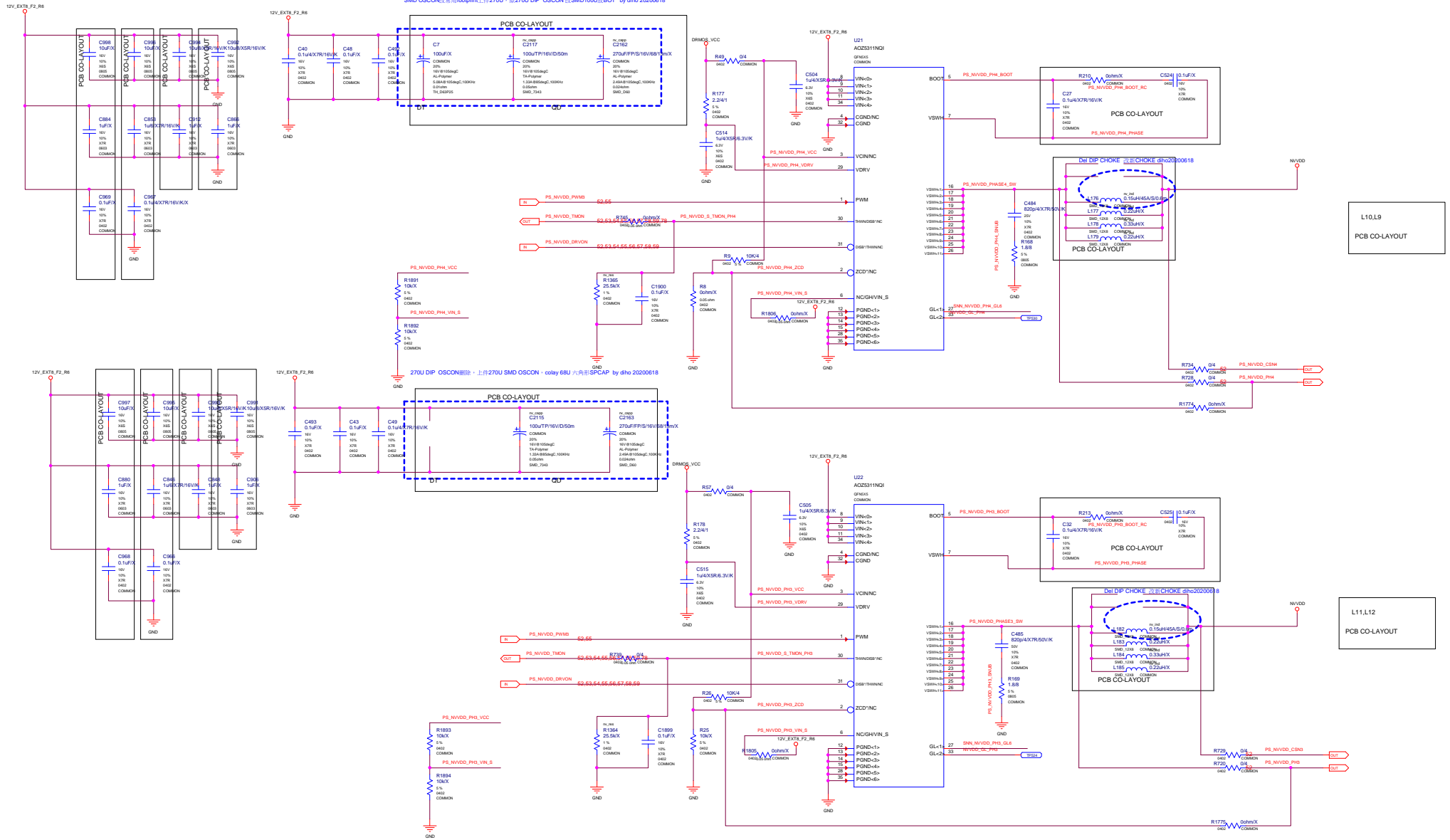
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Size Custom	Document Number GV-N3080AORUSX W-10GD		Rev 1.0
Date: Wednesday, September 30, 2020	Sheet 51	of 79	

PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)

SMD OSCON改常用footprint上件270U，原270U DIP OSCON改SMD100U放BOT by diho 20200618



ASSEMBLY
PAGE DETAIL

PS: NVVDO PH3 (PWM3) and PH4

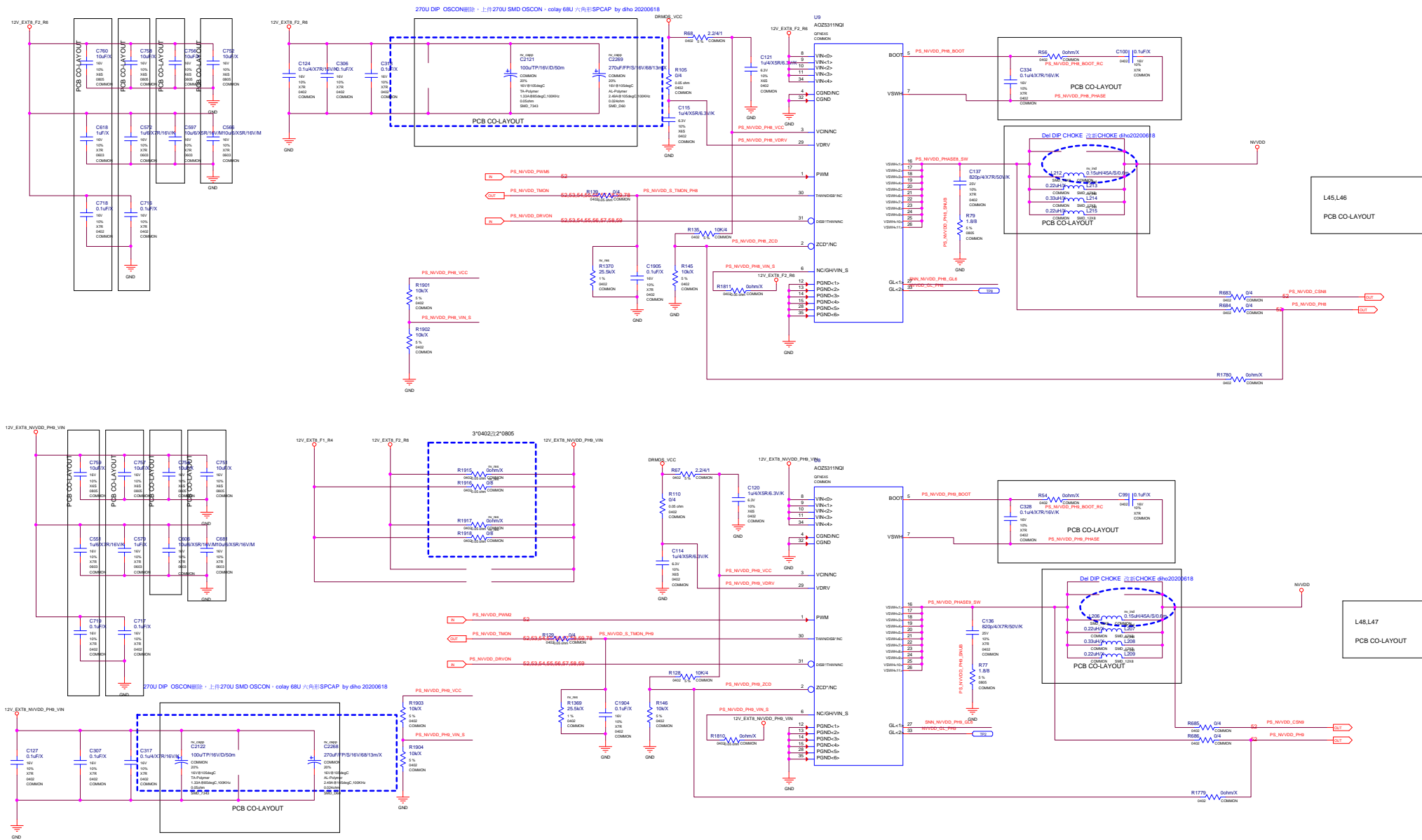
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Title	PS: NVVDD Phase 3,4
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Size	Document Number
Custom	GV-N3080AORUSX W-10GD
Date:	Wednesday, September 30, 2020
Sheet	55 of

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PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



PS: NVVDD PH8(PWM5) and PH9(PWM2)

	A	B	C	D	E	F	G	H
1								
2								
3								
4								
5								

PCB CO-LAYOUT

C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT

C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104, C2138, C2139, C2140, C2141, C2142, C2143, C2144, C2272, C230, C231, C232, C233, C243, C245, C246, C248, C253, C254, C255, C256, C270, C274, C275, C276, C283, C289, C290, C291, C60202, C62004, C62005

C163, C164, C166, C167, C2087, C2105, C2109, C2110, C2111, C224, C225, C261, C268, C269, C60354, C61428, C62, C63, C89, C91, C96

PCB CO-LAYOUT

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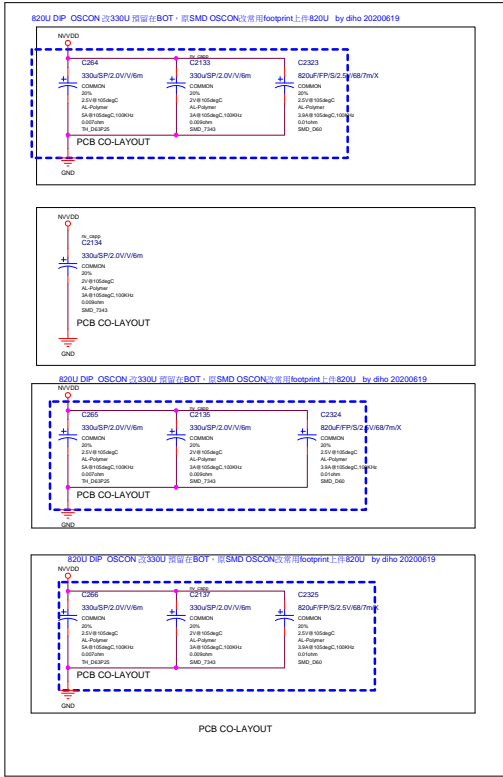
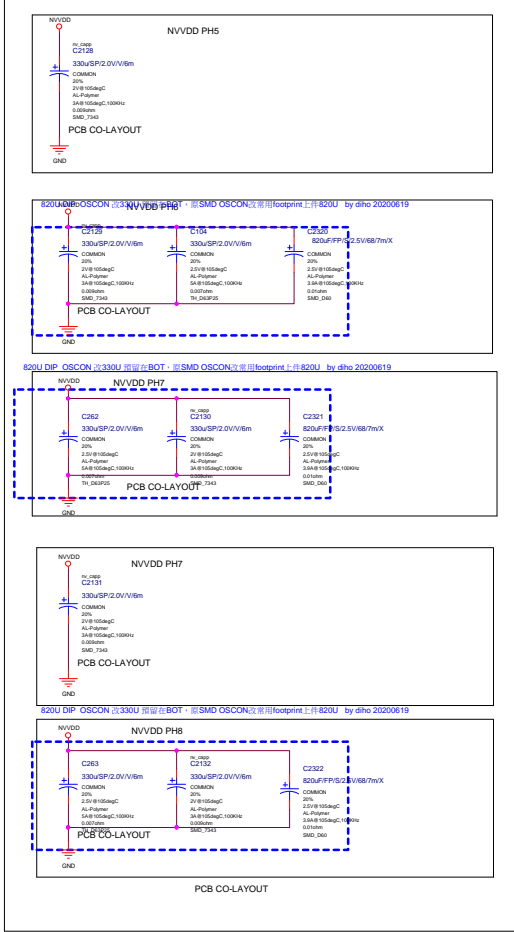
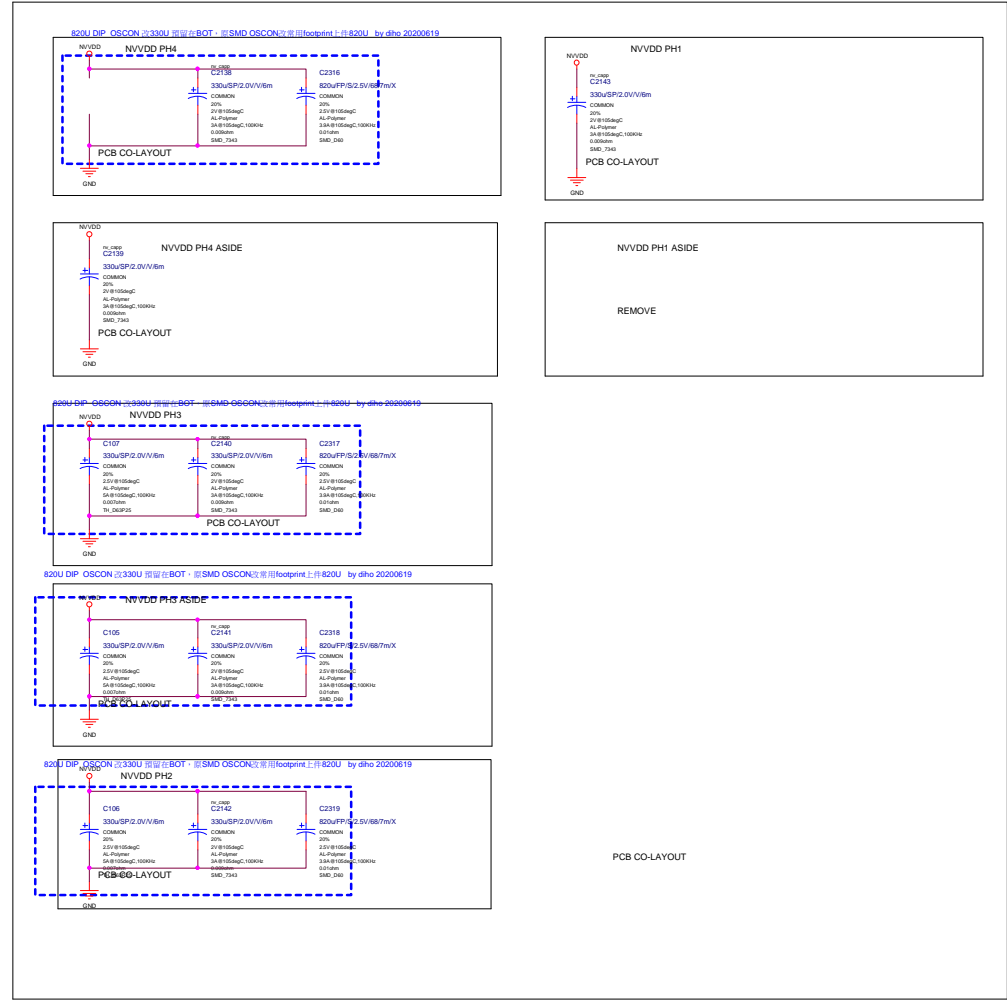
GIGABYTE

COLAY NOTE

Size	Document Number	Rev
Custom	GV-N3080AORUSX W-10GD	1.0
Date: Wednesday, September 30, 2020 8:58 AM Sheet 80 of 79		

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PS: NVVDD OUTPUT CAP(TOP)



PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

1

1

2

2

3

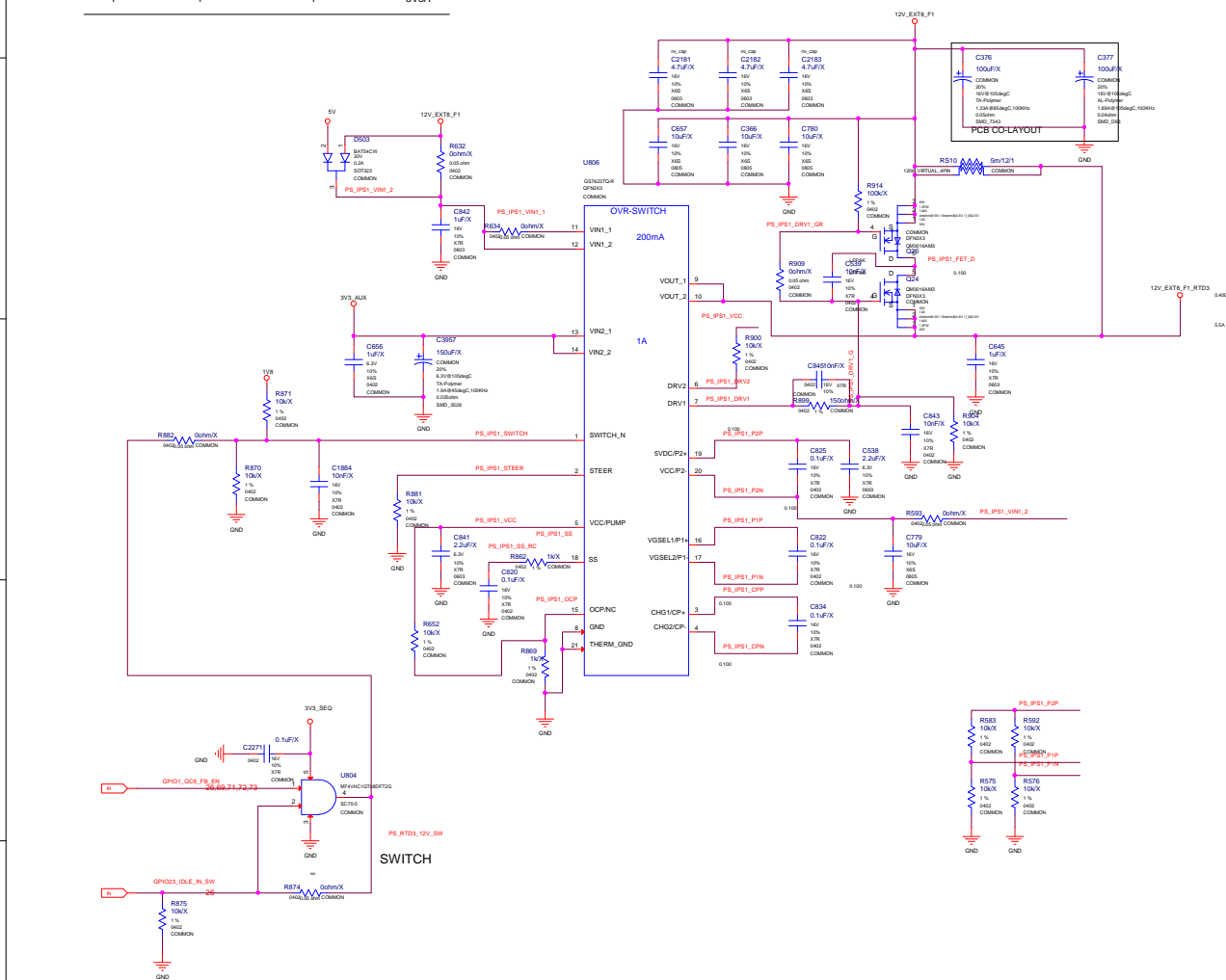
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4

4

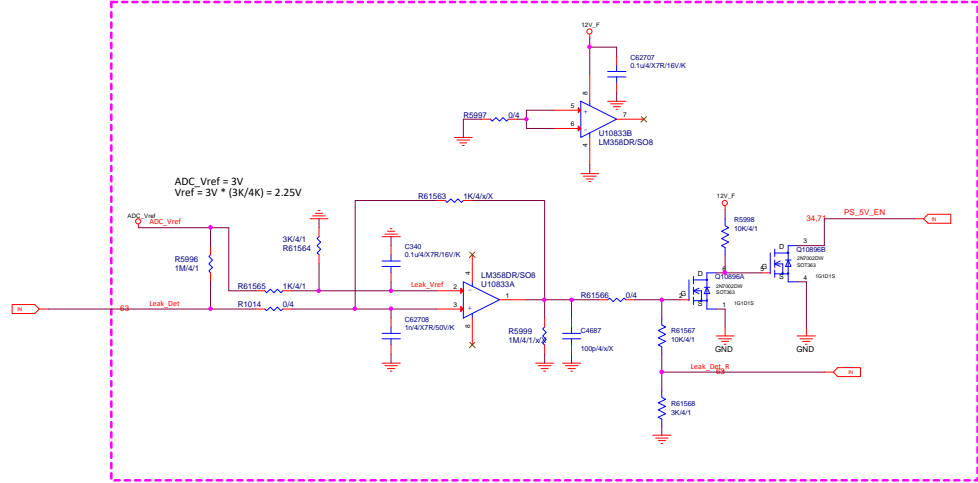
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5

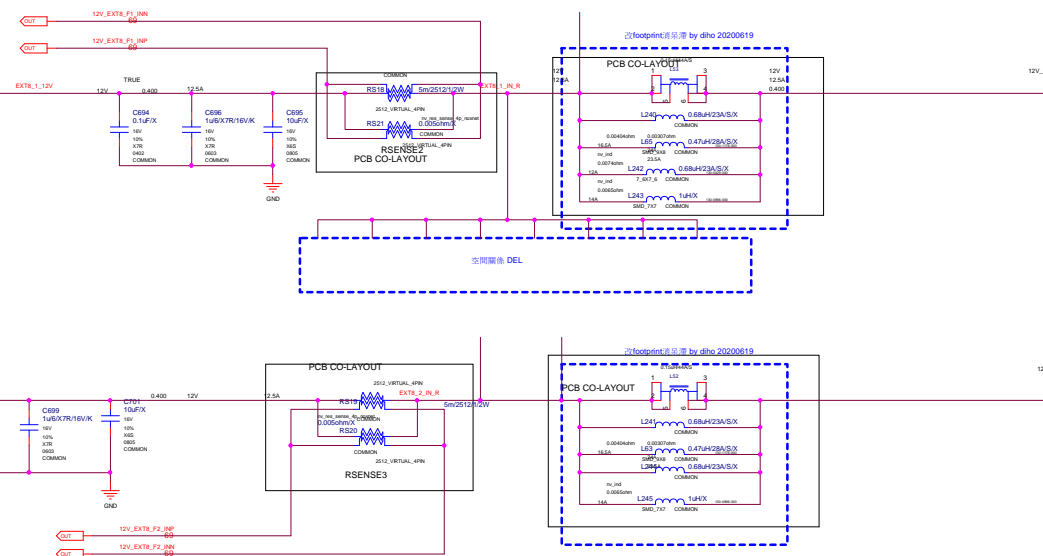
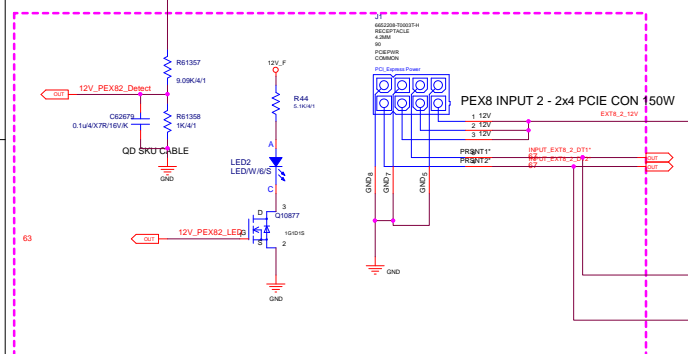
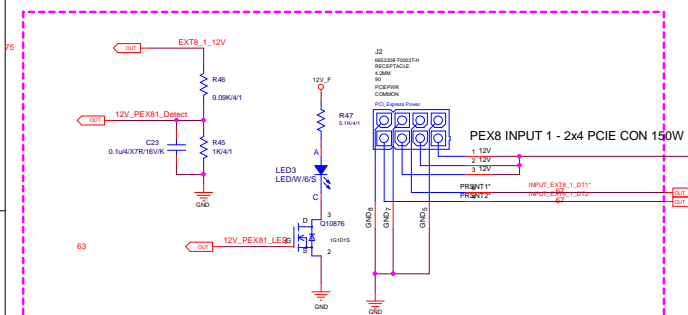
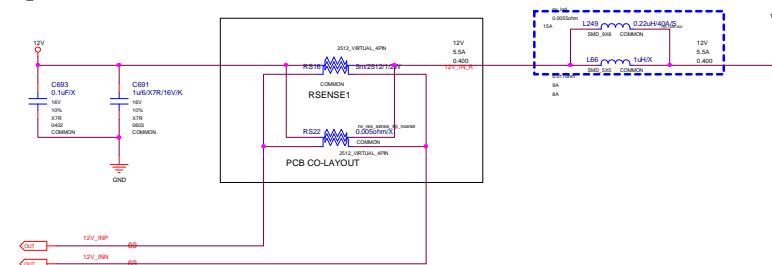
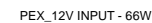
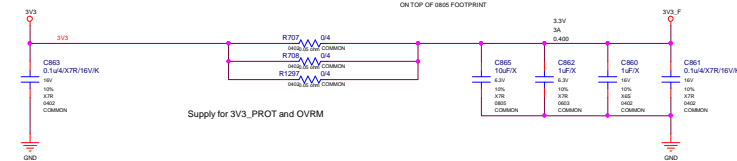
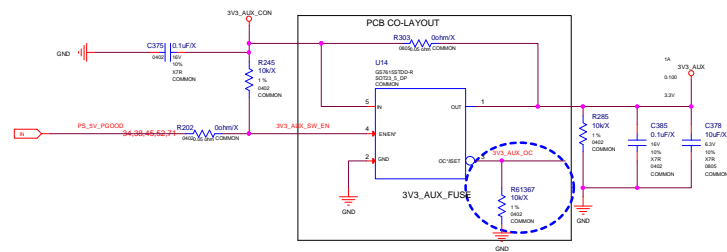


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For Leak detect



PS: Inputs, Filtering, and Monitoring



J24,J25,J26,J27

ASSEMBLY
PAGE DETAIL

PS: INPUTS, FILTERING, and MONITORING

GIGABYTE

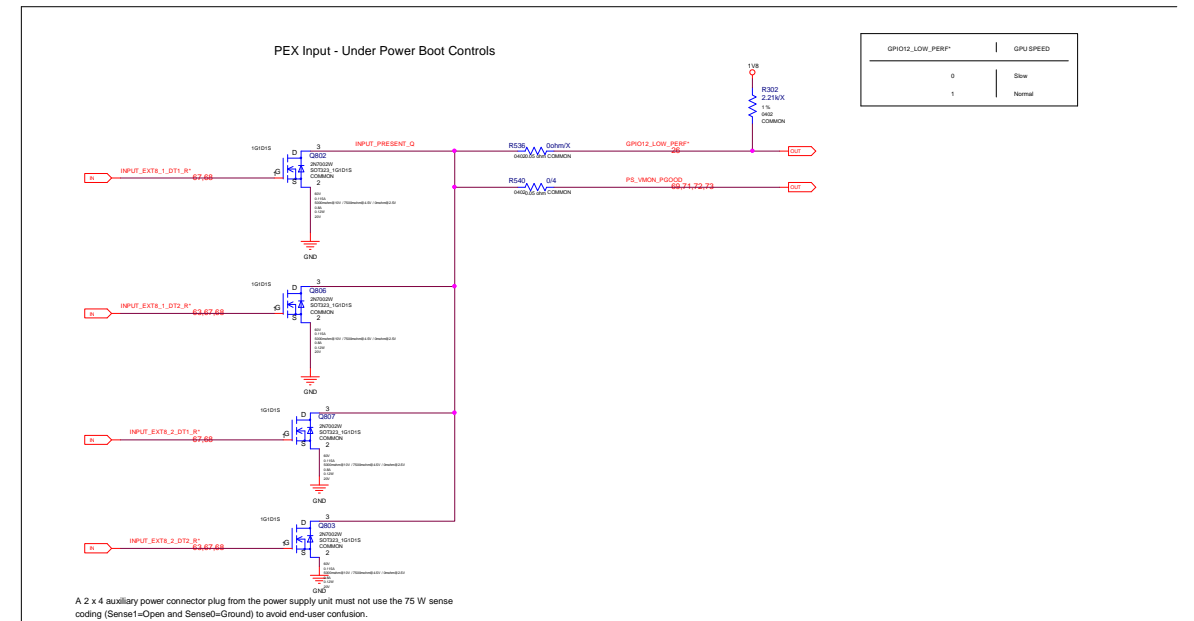
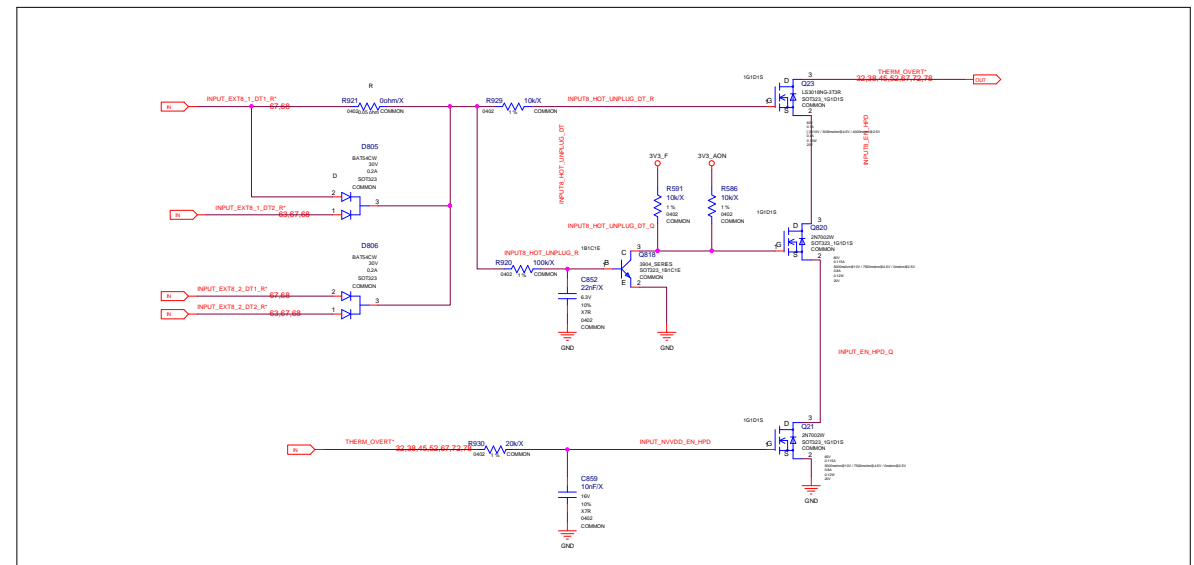
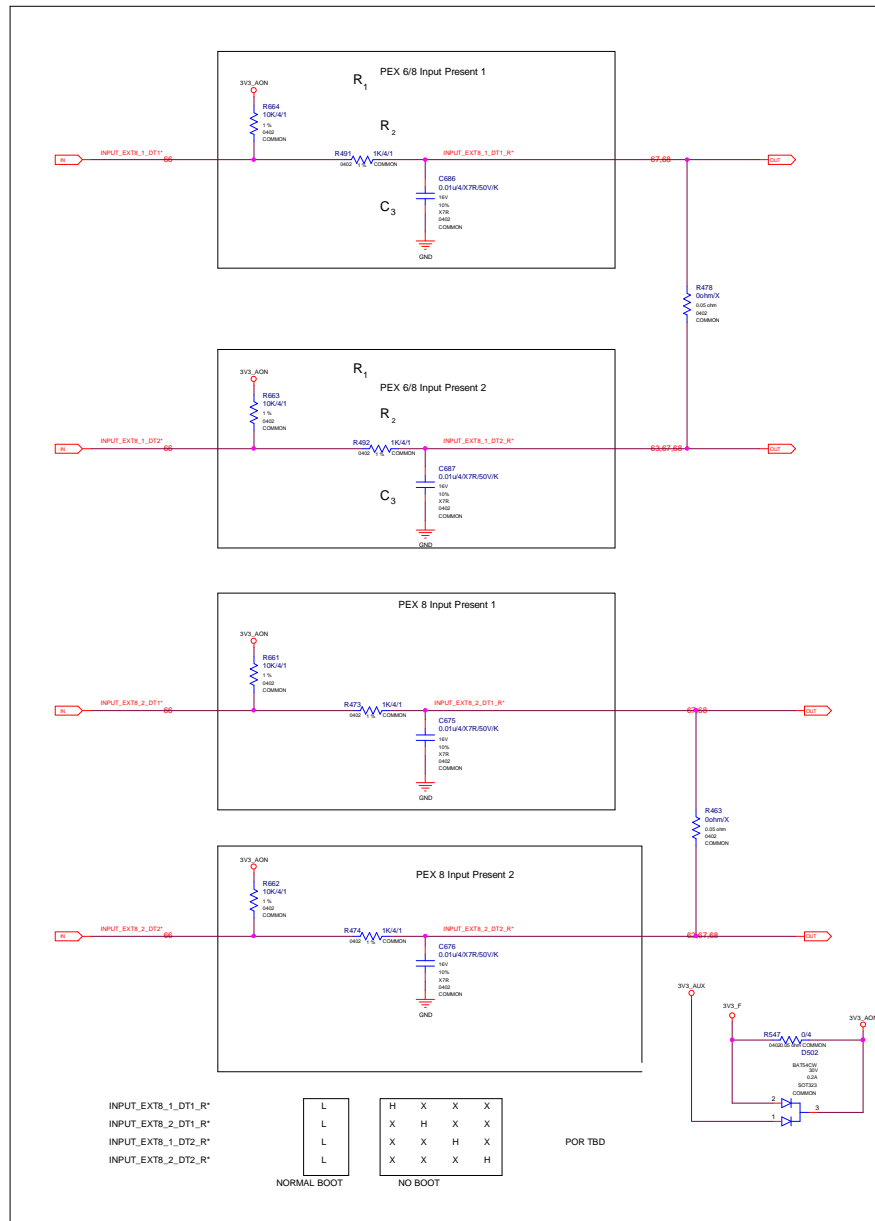
PS: Inputs, Filtering, and Monitoring

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Date: Wednesday, September 30, 2020 Sheet 66 of 70

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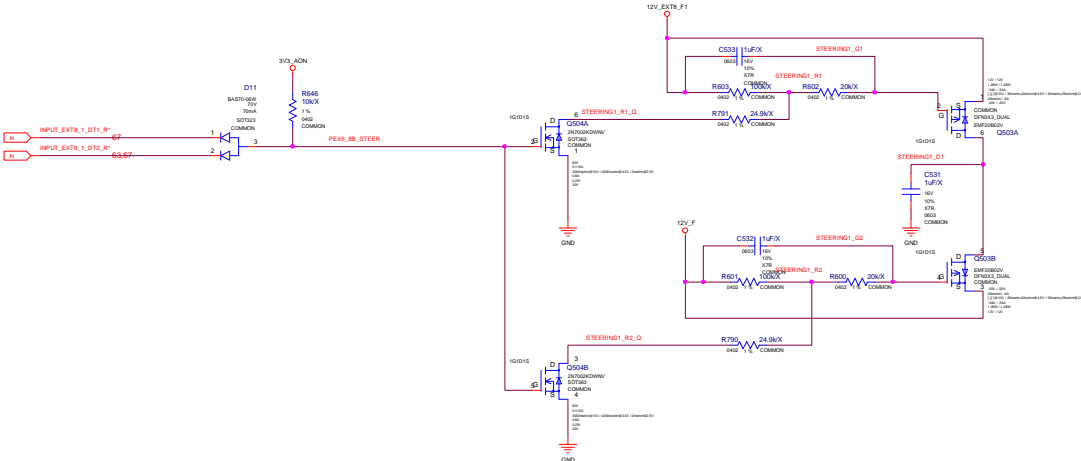
PS: 12V Current Steering & Hot Unplug Detect



PS: Discrete Steering

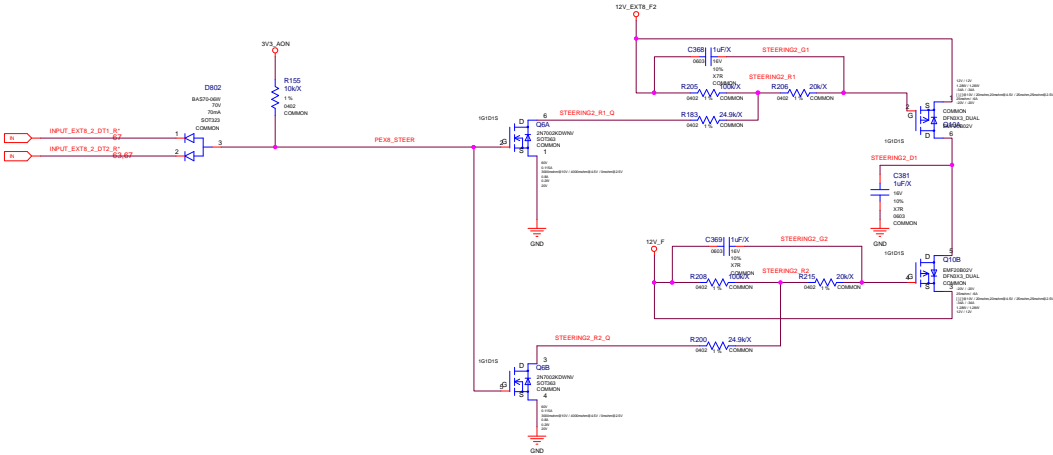
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1

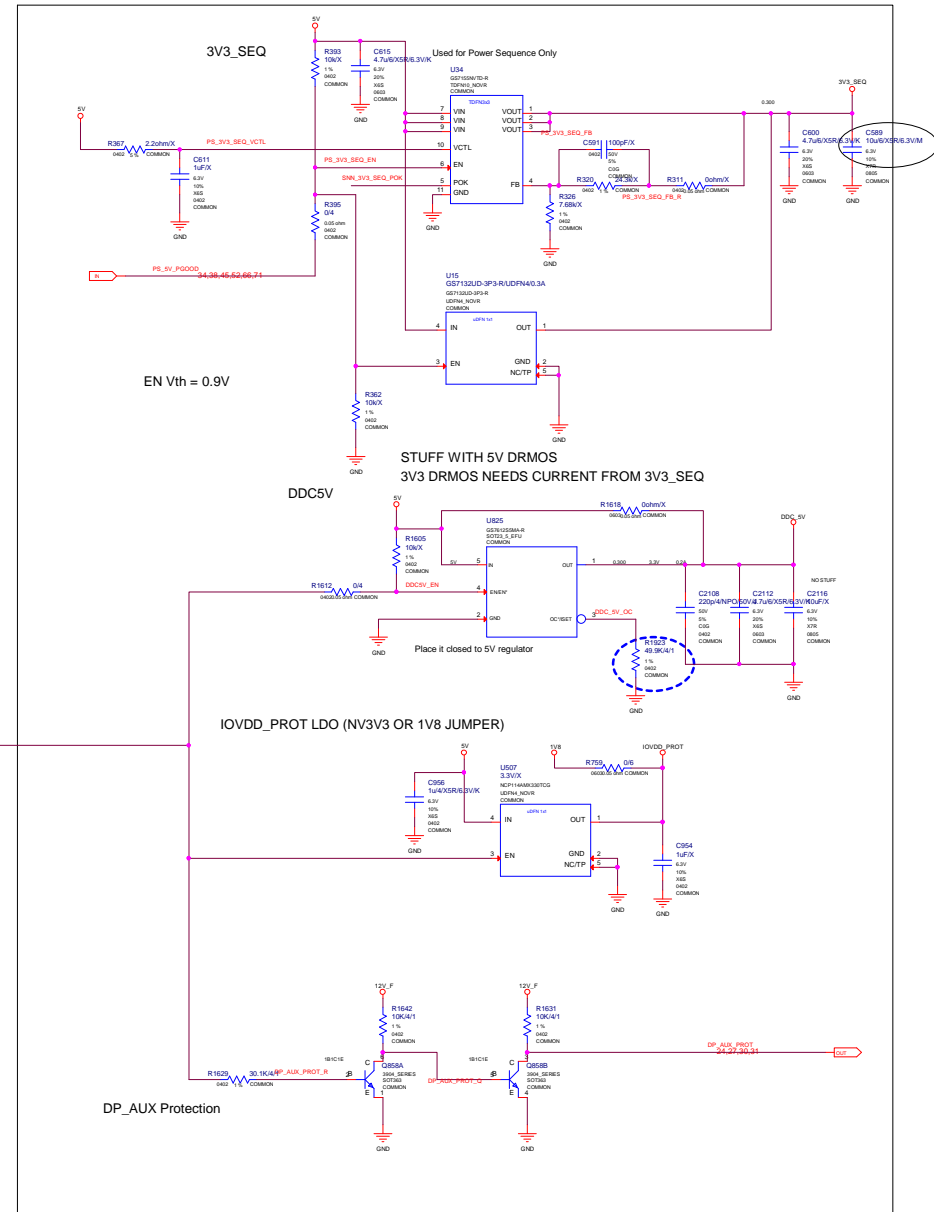
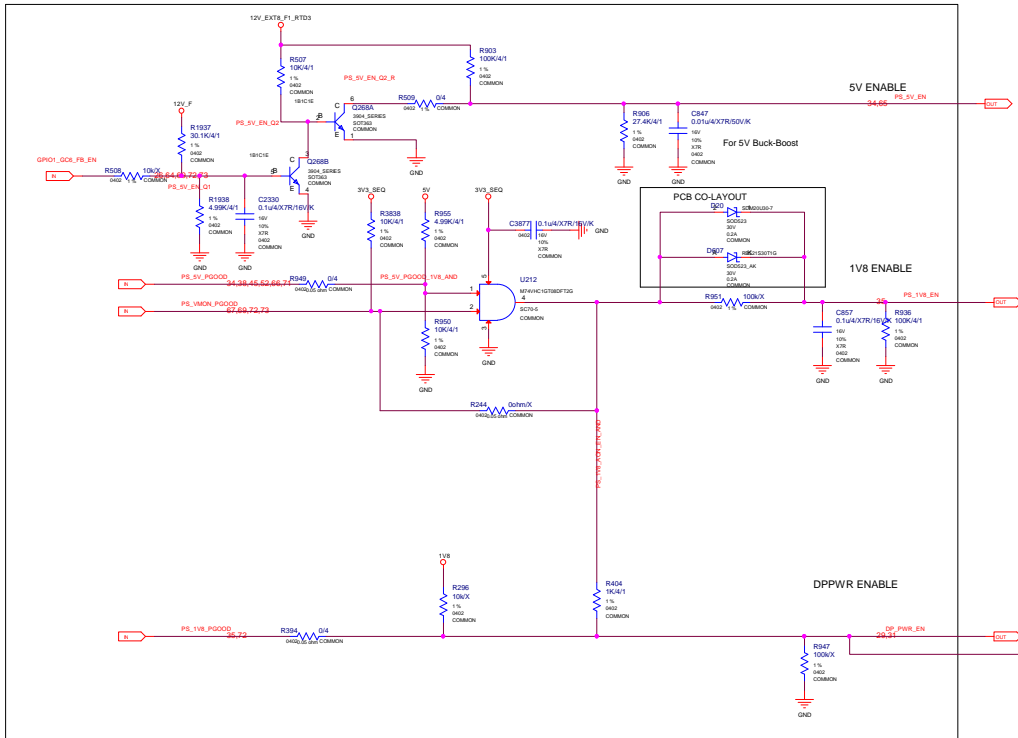


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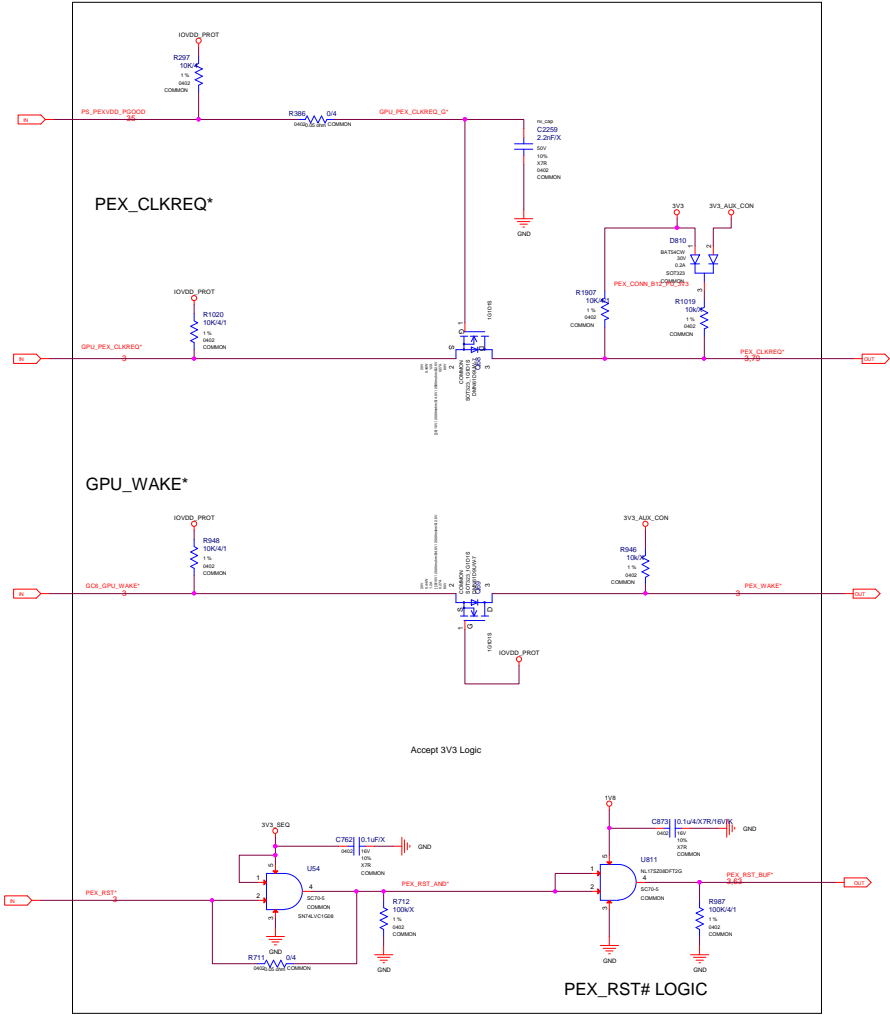
PEX12V AND 12V_EXT8_F2



SEQUENCE:5V,1V8,3V3_SEQ ENABLE



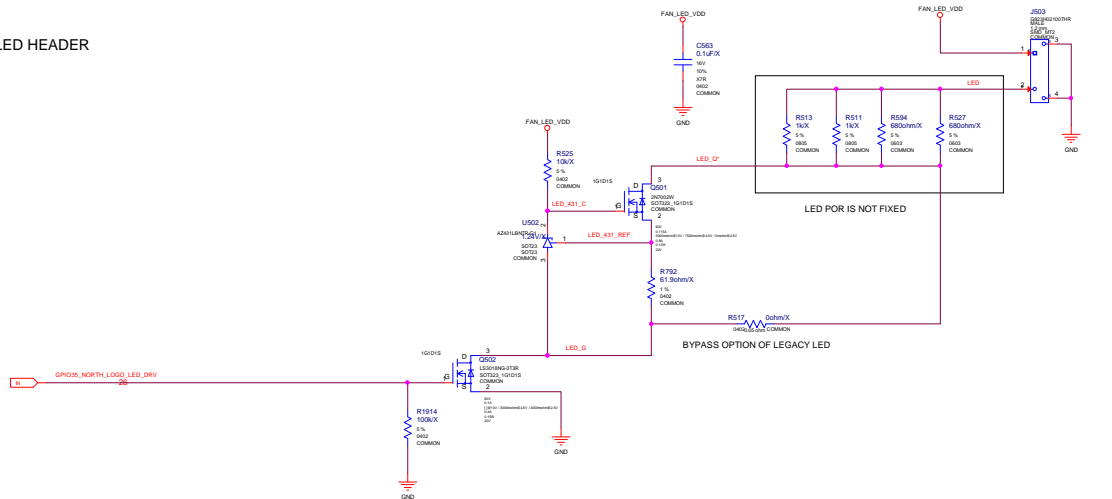
SEQUENCE:MISC



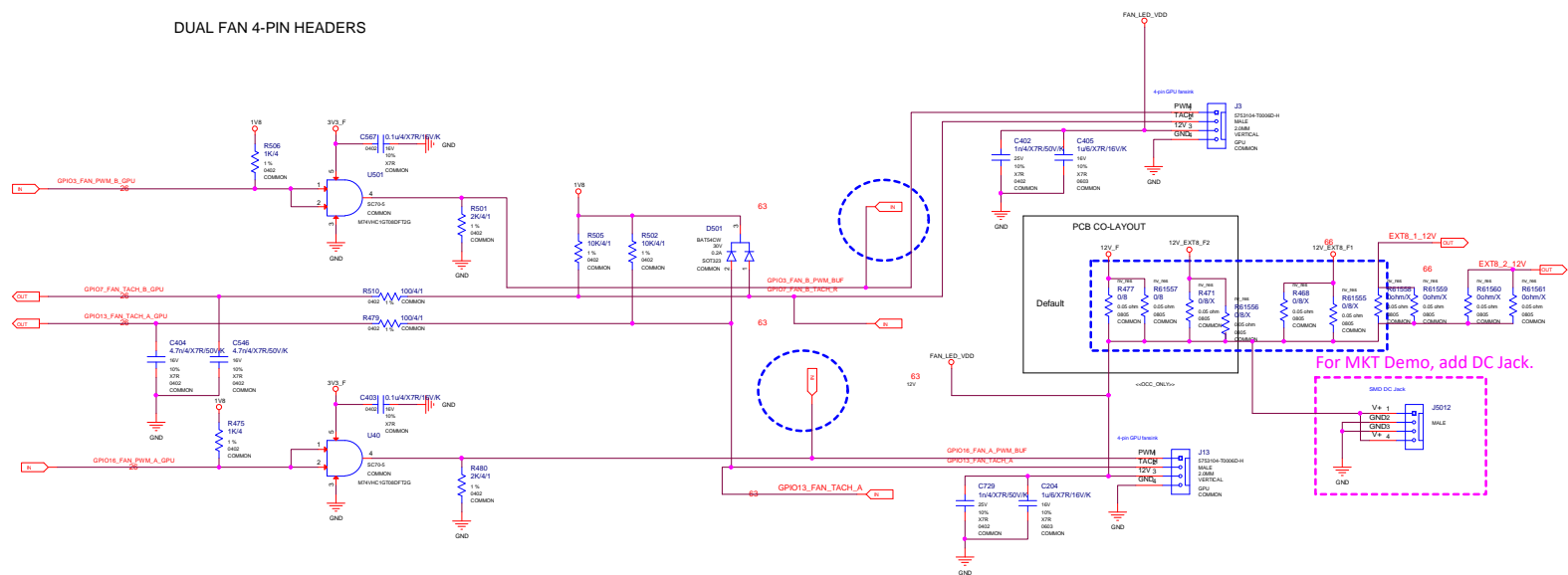
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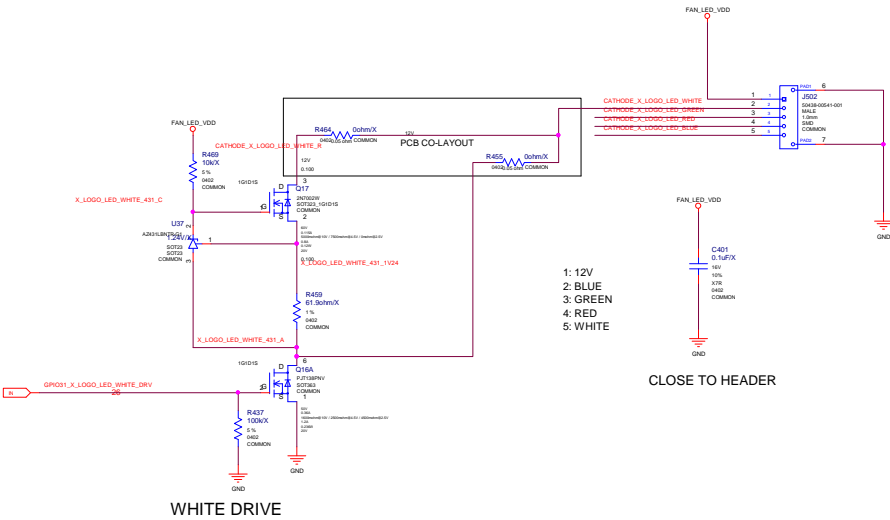
MISC: LED & FAN

2-PIN LED HEADER

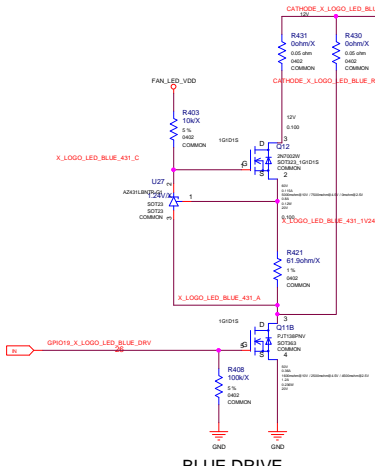
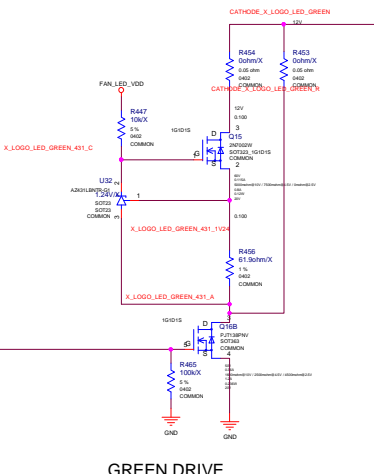
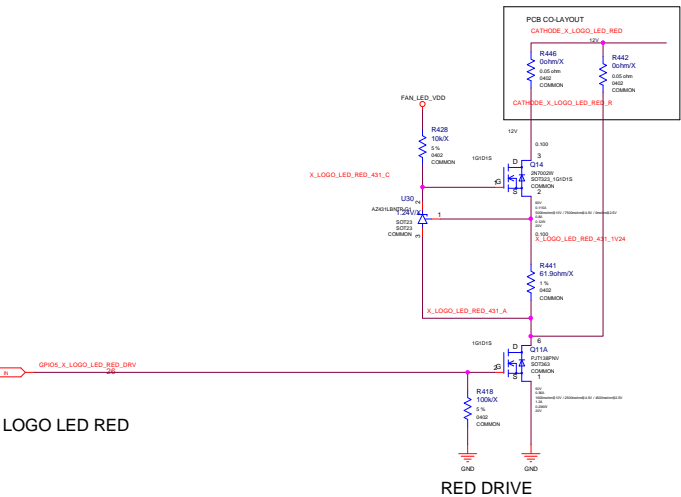


DUAL FAN 4-PIN HEADERS

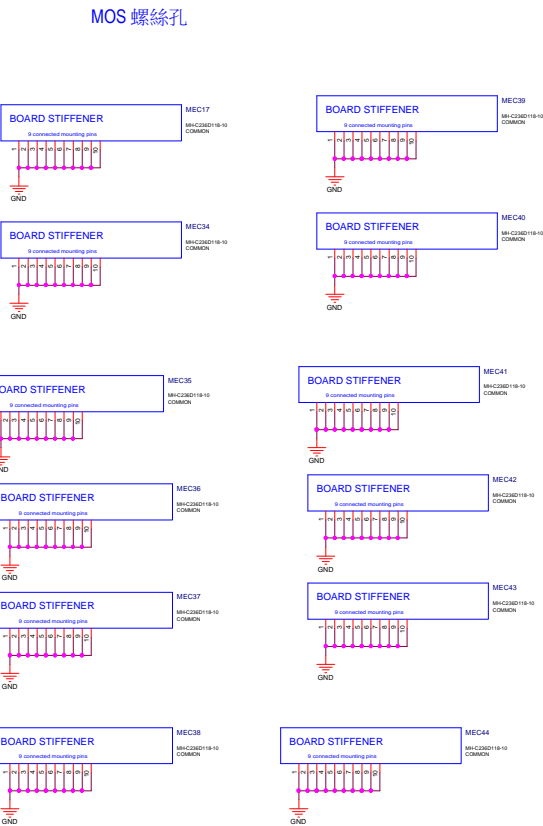
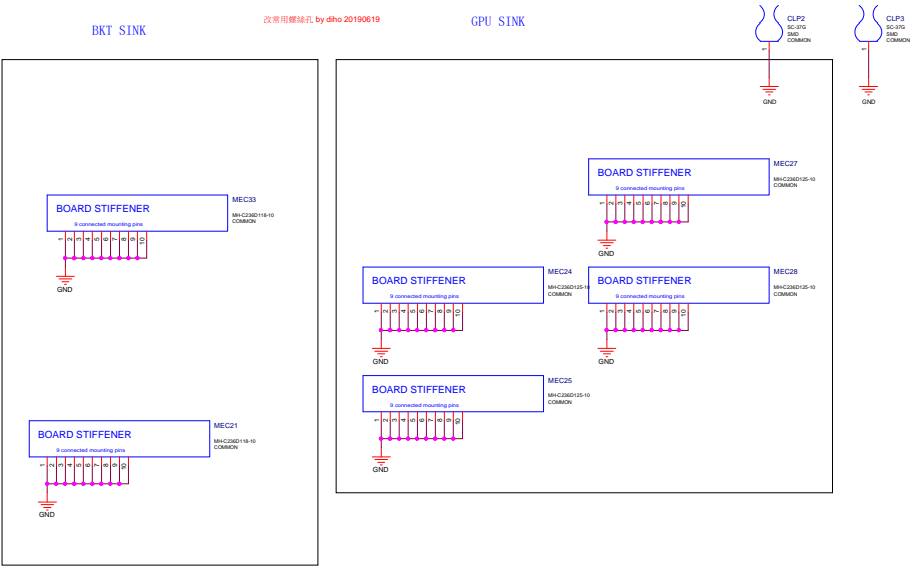




CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALINGN WITH PASH
IF ADDITIONAL POWER CONSUMPTION R
NEEDED, IT SHOULD BE ON LED MOD.



Mechanical: Mounting holes



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VR THERMAL PROTECTION

